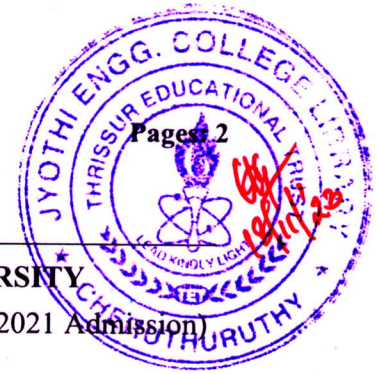Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech (Minor) Degree Examination June 2023 (2021 Admission)

Course Code: MRT282

Course Name: FUNDAMENTALS OF ANALOG AND DIGITAL ELECTRONICS

Max. Marks: 100   Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)   Marks

1	Explain the comparison of BJT and FET	3
2	Explain the construction of MOSFET	3
3	Explain the ideal characteristics of an op amp	3
4	Briefly explain S/H circuit using op amp	3
5	Briefly explain active filters	3
6	Explain lock range and capture range	3
7	State and prove De-Morgan's theorem	3
8	Explain the function of a multiplexer with an example	3
9	Explain the operation of SISO shift register	3
10	Explain the working of Modulo 3 Counter	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Explain the construction and characteristics of JFET	7
	b)	Explain the common emitter configuration of BJT as an amplifier	7
12	a)	Explain Barkhausen criteria	4
	b)	Explain with circuit diagram an RC phase shift oscillator	10

Module -2

13	a)	Differentiate with circuit diagram an inverting and non-inverting amplifier	7
	b)	Explain with necessary figures an ideal differentiator using op amp	7
14	a)	Briefly explain zero crossing detector using op amp	7
	b)	Explain with necessary figures an integrator using op amp	7

Module -3

15 a) Explain the basic building blocks of PLL   10

    b) Comparison between LPF and HPF   4

16 a) Explain the working of a astable multi vibrator using 555 timer   10

    b) Explain the principle of frequency multiplication using PLL   4

Module -4

17 a) Simplify the given expression using k map   9

       $Y=\sum 1,4,8,12,13,15+d (3,14)$

    b) Implement the simplified function using logic gates   4

18 a) Design a four-bit binary to gray code converter   7

    b) Design a full adder using logic gates   7

Module -5

19 a) Explain master slave JK flip flop   7

    b) Design a counter that counts the sequence $y=\sum 0,1,3,5,7,0,1,3,5\ldots\ldots$ 7

20 a) Design a mode 6 synchronous counter   8

    b) Explain the difference between synchronous and asynchronous counter   6

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