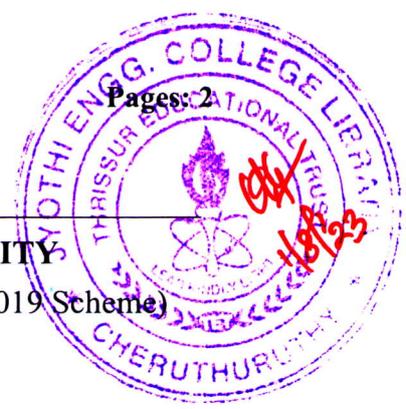


Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R,S) / S2 (PT) (R,S) Examination June 2023 (2019 Scheme)

**Course Code: EET206****Course Name: DIGITAL ELECTRONICS**

Max. Marks: 100

Duration: 3 Hours

PART A*(Answer all questions; each question carries 3 marks)*

Marks

- | | | |
|----|--|---|
| 1 | Convert 10110010 to hexadecimal and Octal | 3 |
| 2 | Draw the truth table and explain the operation of EX-OR and EX-NOR gates | 3 |
| 3 | Get the dual of the expression $AB + \overline{AC} + A\overline{B}C(AB + C) = 1$ | 3 |
| 4 | Derive the expression for sum and carry of a full adder | 3 |
| 5 | Explain a two bit comparator | 3 |
| 6 | Draw the circuit of a 1 to 4 Demultiplexer and explain | 3 |
| 7 | Explain the truth table and excitation table of a JK flip flop | 3 |
| 8 | What are the asynchronous inputs of a flip flop? Why are they called so? | 3 |
| 9 | Draw the state diagram of a three bit binary down counter | 3 |
| 10 | What is FPGA? | 3 |

PART B*(Answer one full question from each module, each question carries 14 marks)***Module -1**

- | | | |
|----|--|---|
| 11 | a) Perform the following (i) 165.875_{10} to binary (ii) $4BAC_{16}$ to binary (iii) 378_{10} to octal | 7 |
| | b) What are universal gates. Why are they called so? | 7 |
| 12 | a) With the help of a neat diagram explain CMOS NAND gate | 7 |
| | b) Describe error detection and correction using parity checking | 7 |

Module -2

- | | | |
|----|--|---|
| 13 | a) Design and set up a half adder/subtractor circuit with mode control. | 7 |
| | b) Obtain the simplified POS expression using K-map – $Y = \sum m(1,3,7,11,15) + d(0,2,4)$ | 7 |
| 14 | a) Using a neat circuit explain a 3 bit carry look ahead adder | 9 |
| | b) Write and explain any five basic laws of Boolean algebra | 5 |

Module -3

- 15 a) Implement $f(x,y,z) = \sum m(1,2,6,7)$ using 4 x 1 MUX 7
b) Explain a 3 to 8 decoder 7
- 16 a) Design and set up a Binary to BCD converter circuit 10
b) How is priority encoder different from encoder 4

Module -4

- 17 a) Draw the logic circuit of SR flip flop and explain it 7
b) What is modulus of a counter. Draw the circuit of an asynchronous decade counter 7
- 18 a) Enumerate the steps for design of a synchronous counter 7
b) Draw the circuit of 4 bit ring counter and give the timing diagram 7

Module -5

- 19 a) Design a 4 bit weighted resistor DAC whose full scale output voltage is -5V. 10
The logic levels are Logic 1 = +5 V and logic 0 = 0 V. What is the output voltage when the input is 1101
- b) Give the Verilog code for AND gate 4
- 20 a) Explain Flash type A/D converter 10
b) Differentiate PAL and PLA 4
