Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech Degree S4 (R, S) / S2 (PT) (R, S) Examination June 2023 (2019 scheme)

Course Code: CST202

Course Name: Computer Organization and Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1		With a neat diagram explain the internal architecture of CPU?	3
2		Enumerate the sequence of actions (control signals) involved in executing an unconditional branch instruction?	3
3		What is micro-operation, With help of examples explain shift micro-operation	3
4		Check the correctens of the following statements and justify your results i)All unifunctional pipeline are static. But all static pipeline are not unifunctional. ii)All dynamic pipelines are multifunctional. But all multifunctional pipeline are not dynamic because different time	3
5		Divide (1000) 2 by (11) 2 using restoring division method.	3
6		With proper example describe about arithmetic pipelining?	3
7		Differentiate between vertical and horizontal microinstructions?	3
8		Draw and discuss about PLA control logic?	3
9		Why dynamic RAMs need constant refreshing? Give the structure also.	3
10		Differentiate about memory mapped I/O and I/O mapped I/O?	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	What do you mean by addressing modes, with proper examples explain in detail about various address modes?	10
	b)	Write down the sequence of actions needed to fetch and execute instruction: STORE R1,[R2]	4
12	a)	Draw the diagram of a multi-bus organization with 3 buses, write the control sequence for the instruction ADD [R1],R2,R3 for the above mentioned multi-bus organization.	9
	b)	What are condition codes, list the different condition codes?	5

Module -2

13	a)	Design an adder circuit with one selection variable S and 2 inputs A and B. When S=0 circuit performs A+B, when S=1 it performs A-B by taking twos complement of B?	9
	b)	Write a short note about accumulator register?	5
14	a)	Give a simple design for generating status bits for an 8-bit ALU?	6
	b)	How do a binary adder circuit can be used for the implementation of logical operation AND, OR, NOT, XOR.	8

Module -3

15	a)	What do you mean by array multiplier, design 3x3 array multiplier and list out its disadvantages?	7
	b)	Explain in detail about pipeline processors?	7
16	a)	Multiply following using booth's multiplication algorithm: -7 and -3	6
	b)	Describe in detail about instruction hazards and their solution?	8

Module -4

17	a)	With a diagram, explain how control signals are generated using hardwired control?	8
	b)	What are the different elements involved in micro-program control unit explain with a neat diagram?	6
18	a)	With the help of a flowchart for sign-magnitude addition/subtraction, explain the steps involved in developing a hardwired control unit?	10
	b)	Discuss about sequence register and decoder method of control organization?	4

Module -5

19	a)	Give the internal organization of 2MX8 memory module using 512 K X8 static memory chips	6
	b)	Explain the hit and miss condition occurring during the read and write operation on cache memory. Also give the importance of dirty bit during the writing operation.	8
20	a)	Differentiate centralized and distributed bus arbitration mechanism used in DMA?	6
	b)	With the help of example, explain different cache mapping functions?	8

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