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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree Supplementary Examination June 2023 (2019 Scheme)

Course Code: EET206

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1		Find the Binary code and Gray code of the number $3A8_{16}$	3
2		Draw the Truth table and explain the operation of Universal Gates	3
3		What is half subtractor. Implement the circuit using logic gates	3
4		Express $AB + A\bar{B}C + B\bar{C}$ as standard SOP expression	3
5		Implement $Y(A,B,C) = \sum m\ (0,1,2,6,7)$ using MUX	3
6		Design a 2 bit magnitude comparator using logic gates.	3
7		Derive the characteristic equation of JK flip flop	3
8		Draw the circuit of 4 bit Johnson counter and give the output table	3
9		With Suitable design diagram , explain PLA	3
10		What is meant by resolution of a DAC	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Perform -25+14 using 1's compliment and 2's compliment method	7
	b)	With a neat diagram explain TTL NAND gate	7
12	a)	Discuss the various methods of representing signed numbers in binary	7
	b)	Compare CMOS logic and TTL	7

Module -2

13	a)	Reduce the expression Y = ∑m(0,1,2,3,5,7,8,9,10,12,13) and show the implementation using NAND gates	7
	b)	Show the implementation of full adder using half adders	7
14	a)	State and prove De Morgan's theorem	6
	b)	Explain the difference between ripple adder and carry look ahead adder with implementation details.	8

Module -3

15	a)	Give the block diagram representation of ALU and explain it	10
	b)	Draw the logic circuit of a 2 to 4 decoder	4
16	a)	Design a logic circuit for even parity generation, Explain the operation.	10
	b)	Draw the logic circuit of 4 to 1 MUX	4

Module -4

17	a)	Convert a SR flip flop to JK flip flop	7
	b)	Realise and explain a 3 bit asynchronous up counter and show the timing diagram	7
18	a)	What is race around condition and how it can be rectified in JK Master Slave F/F	6
	b)	Explain SISO, SIPO, PIPO, PISO registers	8

Module -5

19	a)	Design a synchronous counter that goes through the states 0,3,5,6,0,3,5,6,0,... using T flip flop	7
	b)	Explain a Successive approximation type ADC using a neat diagram	7
20	a)	Write the Verilog code for a half adder	7
	b)	Explain R-2R ladder type of DAC	7

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