

B

02000CST202052104

Pages: 2

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree Supplementary Examination June 2023 (2019 scheme)



Course Code: CST 202

Course Name: Computer Organization and Architecture

Max. Marks: 100

Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

Marks

- | | | |
|----|---|---|
| 1 | Define three, two and one-address instructions with one example for each. | 3 |
| 2 | Why is the Wait-for-Memory-Function-Completed step required when performing memory transfer operations? | 3 |
| 3 | What are the basic components of Register-Transfer Logic method? | 3 |
| 4 | Draw the hardware implementation of a 4-bit combinational shifter. | 3 |
| 5 | Design 3 X 2 array multiplier. | 3 |
| 6 | Explain the logic used behind booth multiplication algorithm | 3 |
| 7 | Give the advantages and disadvantages of hardwired control over microprogrammed control. | 3 |
| 8 | What is a control word? With an example, show how a control word can be defined. | 3 |
| 9 | Differentiate between program-controlled I/O and interrupt-driven I/O. | 3 |
| 10 | Compare temporal locality of reference and spatial locality of reference. | 3 |

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

- | | | |
|----|---|----|
| 11 | a) With a neat diagram, explain the basic operational concepts in transferring data between the processor and the main memory. | 7 |
| | b) What are addressing modes? Explain the different types of addressing modes with examples | 7 |
| 12 | a) Draw the diagram of a single-bus organization of the datapath inside a processor. Give the control sequence for executing the instruction Add [R1], R2 ie, $[R1] \leftarrow [R1] + R2$ in a single-bus organization. | 10 |

02000CST202052104

- b) Give the control sequence for implementing the conditional branch instruction **Branch-on-Negative** in a single bus processor organization. 4

Module -2

- 13 a) Show the hardware implementation of the following conditional control statements 7
T1: $C \leftarrow A$
T2: $C \leftarrow B$, where A, B, C are registers
- b) What is a scratchpad memory? Draw the block diagram of a processor employing scratchpad memory. 7
- 14 a) Design an adder/subtractor circuit with one selection variable s and two inputs A and B. When $s = 0$, the circuit performs $F = A+B$. When $s = 1$, the circuit performs $F = A - B$. 7
- b) Give the hardware design for generating status bits for an 8-bit ALU. 7

Module -3

- 15 a) Draw the hardware arrangement for restoring integer division. Show how the division of 1000 by 11 is performed by restoring integer division.* 10
- b) Show how the multiplication of 1101 and 1011 is performed by a sequential circuit multiplier. 4
- 16 a) Explain the classification of pipeline processors. 10
- b) Write a note on data hazard detection resolution. 4

Module -4

- 17 a) With a block diagram, explain how control signals are generated using hardwired control. 10
- b) Differentiate vertical and horizontal microinstructions. 4
- 18 List the address-sequencing capabilities of a microprogram sequencer. With a suitable block diagram and function table, explain the organization of a typical microprogram sequencer. 14

Module -5

- 19 a) Explain how interrupts can be used for coordinating I/O transfers. 7
- b) Explain how Direct Memory Access technique is used for transferring large blocks of data at high speed. 7
- 20 a) Compare Asynchronous DRAMs and Synchronous DRAMs. 5
- b) Explain the different cache mapping functions with an example for each. 9
