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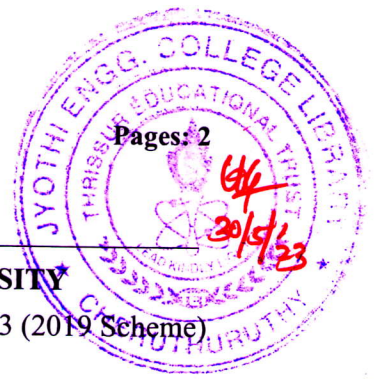
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Reg No.: \_\_\_\_\_

Name: \_\_\_\_\_

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Sixth Semester B.Tech Degree Supplementary Examination May 2023 (2019 Scheme)



Course Code: ECT304

Course Name: VLSI CIRCUIT DESIGN

Max. Marks: 100

Duration: 3 Hours

**PART A**

*Answer all questions, each carries 3 marks.*

		Marks
1	Explain the significance of Moore's law in semiconductor industry	(3)
2	Compare logical and physical design	(3)
3	Implement AND function using NMOS logic	(3)
4	What are the advantages of CMOS logic	(3)
5	What is memory? Distinguish between volatile and non-volatile memory	(3)
6	Draw the circuit of one transistor DRAM cell	(3)
7	What is a carry-bypass adder? Write the expression for delay associated with carry-bypass adder.	(3)
8	Describe the basic functions of an array multiplier	(3)
9	Discuss the term oxidation? What are the advantages of SiO <sub>2</sub>	(3)
10	What are the design rules in VLSI chip design	(3)

**PART B**

*Answer one full question from each module, each carries 14 marks.*

**Module I**

- 11 a) With neat diagram explain ASIC design flow. (8)  
b) Distinguish between Top down and Bottom up approach (6)

**OR**

- 12 a) Explain gate array based ASIC design (8)  
b) What is FPGA? With neat diagram explain the internal architecture of FPGA. (6)

**Module II**

- 13 a) Describe in detail about pass transistor and transmission gate logic (8)  
b) Implement the following using Transmission gates (6)  
i) NAND  
ii) NOR  
iii) XOR

OR

- 14 a) Realize the logic functions using CMOS logic (8)  
(i)  $X = ((A.B) + (C.D))'$   
(ii)  $Y = (A.(B+C.D))$   
b) Explain switching power dissipations in CMOS logic (6)

**Module III**

- 15 a) Design a six transistor SRAM cell. Explain its operation (8)  
b) Explain the basic principle of operation of Domino logic. What are its advantages (6)

OR

- 16 a) Design a 4x4 NOR based MOS ROM Cell array and explain its operation (8)  
b) Describe the principle of operation of Dynamic logic with neat diagram (6)

**Module IV**

- 17 a) Design static CMOS full adder cell with not more than 28 transistors using logic level optimisation (8)  
b) Explain the working of 16-bit carry bypass adder with a neat block diagram (6)

OR

- 18 a) With a diagram illustrate the principle of operation of an 4X4 array multiplier. Show the critical path and also estimate the delay of the multiplier. (8)  
b) Explain the working of 16-bit linear carry adder with a neat block diagram (6)

**Module V**

- 19 a) With necessary diagrams explain Twin Tub process (8)  
b) Illustrate the steps involved in photolithography process with diagrams (6)

OR

- 20 a) Explain Ion implantation technique with neat sketch (8)  
b) Draw the circuit diagram and layout of 2 input NOR gate (6)

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