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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree (S, FE) Examination May 2023 (2015 Scheme)



Course Code: CS202

Course Name: COMPUTER ORGANISATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions, each carries 3 marks

- 1 With the help of an internal block diagram, explain the functions of IR, PC, MAR and MDR. 3
- 2 Register R1 and R2 of a computer contain the values 1200 and 4600. Compute the effective address of the memory operand in the following instructions
1. Add -(R1), R5 2. Store R5, 30(R1), R2 3. Load 20(R1), R5 3
- 3 Write the sequence of control signals to add the contents of register R1 to those register R2 and store the result in register R3, at the execution phase. 3
- 4 Illustrate IEEE standard for single precision floating point numbers 3

PART B

Answer any two questions, each carries 9 marks

- 5 a) What do you mean by byte addressability? What are the two types? 4
- b) With the help of a block diagram write the sequence of operations required for input and output operations 5
- 6 a) Draw the block diagram of single-bus organization of datapath inside a processor. 4
- b) Write the complete sequence of control signals for execution of the instruction Add R2, R1 5
- 7 Draw the circuit arrangement and explain restoring division with an example 9

PART C

Answer all question, each carries 3 marks

- 8 What is the difference between subroutine and Interrupt Service Routine 3
- 9 Differentiate synchronous and asynchronous buses 3
- 10 With the help of a block diagram, explain the working of a single SRAM cell 3
- 11 Briefly explain memory hierarchy. 3

PART D

Answer any two questions, each carries 9 marks

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|----|----|---|---|
| 12 | a) | Briefly explain the registers used in a DMA interface | 3 |
| | b) | What do you mean by bus arbitration? Explain the two methods used | 6 |
| 13 | | Explain the methods for handling multiple Interrupts | 9 |
| 14 | a) | What do you mean by locality of reference? | 2 |
| | b) | Explain different cache memory mapping techniques in detail | 7 |

PART E

Answer any four questions, each carries 10 marks

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|----|----|--|----|
| 15 | | Draw a labelled diagram and explain the bus system for four registers | 10 |
| 16 | a) | Draw the bus organization of four processor registers and ALU through common bus. | 5 |
| | b) | Design an adder/subtractor circuit with one selection variable s and two inputs A and B . When $s=0$ the circuit performs addition of inputs. When $s=1$ the circuit performs subtraction. | 5 |
| 17 | a) | With the help of a simple diagram explain the design of a 8-bit ALU with a 4-bit status register | 5 |
| | b) | Design a 4-bit combinational logic shifter which performs transfer, shift right, shift left and transfer zeros. The circuit is constructed with 4 X1 multiplexers with two selection variables $H1$ and $H0$. | 5 |
| 18 | a) | What do you mean by hardwired control? | 2 |
| | b) | With the help of a detailed diagram explain the hardwired control unit organization. | 8 |
| 19 | a) | What is a Control Word? | 2 |
| | b) | Draw and explain the microprogrammed control unit | 8 |
| 20 | a) | Briefly explain vertical and horizontal microinstructions | 4 |
| | b) | Define the following terms associated with microprogrammed control unit: i). Microroutine ii)Microinstruction iii) Control Memory iv)Micro Program Counter | 6 |
