Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fifth Semester B.Tech (Hons.) Degree Examination December 2022 (2020 Admn.)

Course Code: ECT 393
Course Name: FPGA BASED SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks) Marks

1		What is Behavioural Modelling in Verilog?	3
2		What is State Machine Design?	3
3		What are the limitations of FPGA?	3
4		What is a Complex Programmable Logic Device?	3
5		What is meant by configurable logic block?	3
6		Compare coarse and fine grained FPGA architecture.	3
7		What is placement and routing in FPGA?	3
8		What are the benefits of FPGAs in DSP design?	3
9		List different commercially available FPGAs.	3
10		Differentiate combinational circuit with sequential circuit.	3

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

11	a)	Write the Verilog code for a 4:1 multiplexer using behavioural model. Also write truth table and draw schematic.	8
	b)	Write the test bench for 4:1 multiplexer using Verilog.	6
12	a)	Design Verilog code for J-K Flip Flop using behavioural model. Also write truth table and draw schematic.	8
	b)	Explain behavioral modelling with an example.	6

Module -2

13	a)	Draw the structure of PLA and explain it.	5
	b)	Implement the following Boolean expressions using a suitable PLA.	9

$A(x,y,z) = \sum m(1,2,4,6)$. $B(x,y,z) = \sum m(0,1,6,7)$.

$C(x,y,z) = \sum m(2,6)$. $D(x,y,z) = \sum m(1,2,3,5,7)$.

14	a)	Comparison between PROM, PLA and PAL	6
	b)	Implement the following Boolean function using PAL.	8

$F_1(A,B,C) = (1, 2, 4, 5, 7)$. $F_2(A,B,C) = (0, 1, 3, 5, 7)$

Module -3

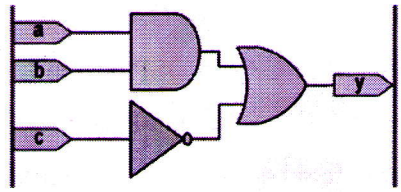
15	a)	With neat diagram explain the internal architecture of FPGA.	14
16	a)	Explain Logic block with neat diagram.	7
	b)	Draw and explain I/O block architecture of FPGA.	7

Module -4

17	a)	Explain in detail three major classes of placement in FPGA.	10
	b)	Explain the placement issues in FPGA.	4
18	a)	With neat diagram explain different Programmable interconnections in FPGA	8
	b)	Explain FPGA Routing Techniques.	6

Module -5

19	a)	What is LUTs in FPGA? Design and implement the following combinational circuit using LUTs in FPGA.	7



	b)	Explain with diagram, how to implement an 8 bit adder using 8 bit LUTs and 4 bit LUTs.	7
20	a)	With neat diagram explain the architecture of Xilinx Virtex.	14

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