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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Seventh Semester B.Tech Degree (S, FE) Examination January 2023 (2015 Scheme)

Course Code: CS405

Course Name: Computer System Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks.

		Marks
1	State Amdahl's law. Assume we are considering an enhancement to the processor of a server. The new CPU is 10 times faster. The server is an I/O bound server, so 60% time waiting for I/O. What is the overall speedup?	(4)
2	With a neat sketch give the details of a vector processor.	(4)
3	Distinguish between multiprocessor and multicomputers.	(4)
4	Discuss about hardware synchronization problem.	(4)
5	Explain hierarchical bus system.	(4)
6	Explain chained cache coherence protocol.	(4)
7	How internal data forwarding improves the performance of a pipelined system?	(4)
8	Define data hazard. What are the three types of data hazards?	(4)
9	Explain the Release Consistency model.	(4)
10	Discuss the principle of multithreading.	(4)

PART B

Answer any two full questions, each carries 9 marks.

11	a)	Consider the execution of an object code with 300,000 instructions on a 400-MHz processor. The program consists of four major types of instructions. The instruction mix and number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment.	(6)

Instruction type	CPI	Instruction mix
Arithmetic and logic	2	52%
Load/store with cache hit	4	18%
Branch	6	20%
Memory reference with cache miss	8	10%

(i) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.

(ii) Calculate the corresponding MIPS rate based on obtained CPI

b) State the Bernstein's conditions to detect parallelism among a set of processes. (3)

12 a) Explain memory hierarchy. (3)

b) Explain Flynn's classification of computer architecture with diagrams. (6)

13 a) Differentiate CISC and RISC architecture. (4)

b) Compare Superscalar and VLIW architectures. (5)

PART C

Answer any two full questions, each carries 9 marks.

14 a) Consider the following reservation table for a four stage pipeline with a clock cycle τ=20ns.

	1	2	3	4	5	6
S1	x					x
S2		x		x		
S3			x			
S4				x	x	

(a) What are the forbidden latencies and the initial collision vector? (2)

(b) Draw the state transition diagram for scheduling the pipeline. (3)

(c) Determine the MAL associated with the shortest greedy cycle. (2)

(d) Determine the pipeline throughput corresponding to the MAL and given τ. (2)

15 a) Explain different flow control strategies. (4)

b) Differentiate between write invalidate snoopy protocol with write through and write back cache policies. (5)

16 a) Discuss the structure of multiport memory with a neat diagram. (3)

b) Describe a crossbar network. Explain about the design of a crosspoint switch with a neat diagram. (6)

PART D

Answer any two full questions, each carries 12 marks.

17 a) Explain different context switching policies. (4)

b) Write down the mechanisms for improving instruction pipelining. (8)

18 a) Differentiate between inorder and out of order issue processor. (4)

b) Describe about the two types of latency problems in multithreading. (4)

c) Define the steps in instruction pipelining. (4)

19 a) Describe the two solutions for asynchrony problem. (6)

b) Outline the latency hiding mechanisms. (6)

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