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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Regular and Supplementary Examination December 2022 (2019 Scheme)

Course Code: RAT205

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1 Convert the hexadecimal number $(A3.EF)_{16}$ into binary and octal. (3)

2 Draw the circuit diagram of a CMOS NAND Gate. (3)

3 Prove that A'B'C' + A'BC' + AB'C' + ABC' = C' using Boolean Algebra. (3)

4 Explain the working of a half adder with truth table and circuit diagram. (3)

5 Derive the characteristic equation of a T flipflop. (3)

6 Distinguish between asynchronous and synchronous counters. (3)

7 Explain the terms resolution and accuracy of an A/D Converter. (3)

8 Compute the minimum number of flipflops required to design a mod 12 ring counter and a mod 12 binary counter. (3)

9 Distinguish between SRAM and DRAM. (3)

10 Write the Verilog Code for a D Flipflop. (3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11 (a) Perform unsigned binary subtraction $(1000)_2$ - $(1010)_2$ using 1's complement and 2's complement method. (7)

(b) Explain the working of a typical TTL NAND gate with necessary table and circuit diagram. (7)

12 (a) Which are the universal gates? Realise basic gates using universal gates. (7)

(b) Convert the following : (7)

(i) $(1001011)_{gray}$ = ( )$_2$ (ii) $(630.4)_8$ = ( )$_{10}$ (iii) $(153.6875)_{10}$ = ( )$_8$

(iv) $(76)_{10}$ = ( )$_{gray}$

Module 2

13 (a) Simplify the Boolean expression F(A,B,C,D) = ∑m(1, 3, 5, 7, 8, 9, 12, 13) using K map (7)

(b) Describe the working of a 4:1 multiplexer with necessary equation, truth table and logic diagram. (7)

14 (a) Obtain the minimal product of sums expression for the function F(A,B,C,D) = Π(4, 5, 6, 8, 9, 12, 13, 14) with don't cares (0, 1) (7)

(b) Explain the working of a four-bit carry look ahead adder with necessary equations and diagram. (7)

Module 3

15 (a) Explain with diagram the working of a master slave JK Flipflop. (7)

(b) Convert a T Flipflop into a JK Flipflop. (7)

16 (a) Design a mod 6 asynchronous up counter with circuit and timing diagram. (7)

(b) Describe with diagram the working of a 4-bit parallel in serial out (PISO) Shift Register. (7)

Module 4

17 (a) Explain the working of a 4-bit Johnson Counter with circuit and timing diagram. (7)

(b) Describe with diagram the operation of a Weighted Resistor DAC. (7)

18 (a) Design a 3-bit synchronous binary up counter using T flip flop. (7)

(b) Explain with diagram the working of a Successive Approximation Type A/D Converter. (7)

Module 5

19 (a) Explain the read and write operations of a basic DRAM cell with necessary diagrams. (7)

(b) Write the Verilog code for a full adder. (7)

20 (a) Describe with diagram the working of a PROM. (7)

(b) Explain the difference between PLA and PAL with necessary diagrams. (7)