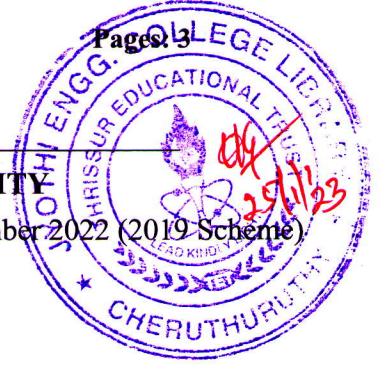


Reg No.: _____

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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Regular and Supplementary Examination December 2022 (2019 Scheme)

**Course Code: EET205****Course Name: ANALOG ELECTRONICS**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer all questions. Each question carries 3 marks*

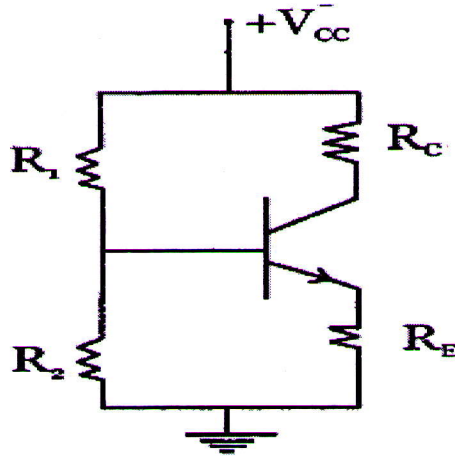
Marks

- 1 Explain the significance in the proper selection of operating point for a CE Amplifier. What are the main factors affecting its stability? (3)
- 2 A base bias circuit for CE amplifier has dc supply (V_{CC}) = 15 V, Collector resistance (R_C)=1.8 k Ω and Resistance connected to base (R_B)=120 k Ω . Assuming Base emitter voltage (V_{BE})=0.7V and $h_{FE} = 50$. Determine operating point parameters I_C and V_{CE} . (3)
- 3 Draw a neat typical output characteristics (I_D vs V_{DS}) of JFET for variations in gate source voltage (V_{GS}) and clearly marking the various regions, Knee point and breakdown point. (3)
- 4 Draw and explain the hybrid pi model of CE amplifier. (3)
- 5 Compare the advantage and drawback of class-B power amplifier over class-A due to the location of operating point. (3)
- 6 Explain Barkhausen criteria for sustained oscillations (3)
- 7 Explain the following terms regarding an op-amp (3)
 - (i) CMRR, (ii) Slew rate
- 8 List any six characteristics of an ideal operational amplifier. (3)
- 9 Draw the circuit diagram of an ideal differentiator and derive the expression for output voltage (3)
- 10 With neat circuit diagram and waveforms, explain zero crossing detector. (3)

PART B*Answer any one full question from each module. Each question carries 14 marks***Module 1**

- 11 (a) Obtain the operating point (I_C and V_{CE} values) sent by a Voltage divider bias circuit for npn CE transistor with V_{BE} =0.7 V and $\beta = 50$. Given V_{CC} is 18 V (9)

supply, $R_C = 5.6 \text{ k}\Omega$, $R_E = 1.2 \text{ k}\Omega$, $R_1 = 82 \text{ k}\Omega$, $R_2 = 22 \text{ k}\Omega$. Also find the Stability factor.



- (b) Explain the role of coupling and emitter bypass capacitor in CE amplifier circuit? How is amplification affected if emitter bypass capacitor is removed from the circuit? (5)
- 12 (a) Obtain the expressions for current gain, input impedance, voltage gain and output impedance using h-parameter equivalent circuit of CE amplifier (9)
- (b) Explain the diode compensation technique adopted in CE amplifier for stability against variations of reverse saturation current (I_{CO}) (5)

Module 2

- 13 (a) A JFET has pinched-off voltage (V_p) of -4.5 V , with maximum saturation current (I_{DSS}) at 10 mA and drain-source current (I_{DS}) at 2.5 mA . Determine the transconductance. (7)
- (b) Draw the equivalent circuit and derive expression for (i) input impedance (ii) Current Gain (iii) Voltage gain and (iv) Output impedance of the Common Drain JFET amplifier (7)
- 14 (a) With the help of diagrams, Explain the constructional features and working of n-channel JFET (7)
- (b) Draw the frequency response characteristics of CE amplifier and explain the significance of corner frequency on output gain and power? Differentiate the capacitances influencing the response during low and high frequency regions. (7)

Module 3

- 15 (a) With the help of neat figures, explain the operation of RC phase shift oscillator using BJT amplifier. Mention the conditions for ensuring sustained oscillations in it. (9)
- (b) Obtain the maximum theoretical efficiency of Class-A power Amplifier. (5)
- 16 (a) With the help of neat figures, explain the operation of Colpitt's oscillator. What are the factors to be considered for ensuring sustained oscillations in it? (9)
- (b) Draw the circuit diagram of a transformer coupled two stage amplifier. What are the advantages and drawbacks of transformer coupling? (5)

Module 4

- 17 (a) How do the open-loop voltage gain and closed loop voltage gain of an op-amp differ? Derive the gain of inverting amplifier using OpAmp. (9)
- (b) What is meant by an instrumentation amplifier. List its main features (5)
- 18 (a) Compare the Ideal and Practical characteristics of an op-amp. Derive the output voltage equation of difference amplifier circuit using Opamps. (7)
- (b) Design an adder circuit using an op-amp to get the output expressions as (7)
- $V_{out} = - (V_1 + 5V_2 + 25V_3)$, where V_1 , V_2 and V_3 are the inputs. Given that $R_f = 50$ k Ω .

Module 5

- 19 (a) With the help of a neat diagram explain the operation of monostable multivibrator using 555 IC? (8)
- (b) Draw the circuit diagram and explain the working of a ramp generator using OpAmp? (6)
- 20 (a) Draw and explain the operation of a triangular wave generator using op-amp. (7)
- (b) Draw the circuit diagram of astable multivibrator using 555 timer IC? (7)
- Determine the positive pulse width, negative pulse width, total time period and free running frequency for an astable multivibrator using 555 timer IC. Given $R_A = 4.7$ k Ω , $R_B = 1$ k Ω and $C = 1$ μ F