

C

0800MRT203122101



Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Regular and Supplementary Examination December 2022 (2019 Scheme)

Course Code: MRT203

Course Name: ANALOG AND DIGITAL ELECTRONICS

Max. Marks: 100

Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks

- | | Marks |
|---|-------|
| 1 What are the conditions for sustained oscillations? | (3) |
| 2 Explain the effect of negative feedback in amplifiers | (3) |
| 3 State characteristics of comparators | (3) |
| 4 Derive the output voltage equation of basic Integrator circuits | (3) |
| 5 Compare Active Filter and Passive Filter | (3) |
| 6 Draw and discuss block diagram of PLL | (3) |
| 7 Why NAND and NOR are called universal gates? | (3) |
| 8 Explain code converters. Write one example of each | (3) |
| 9 What is race around condition? How it is rectified | (3) |
| 10 Compare Asynchronous and Synchronous Counters | (3) |

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

- | | |
|---|-----|
| 11. a) Classify power amplifiers. Write note on Class A power amplifier | (7) |
| b) Explain working of N Channel JFET | (7) |
| 12 a) Explain the working of Hartley oscillator. | (7) |
| b) Classify the types of negative feedback & explain each in brief. | (7) |

Module 2

- | | |
|---|------|
| 13 a) Write the characteristics of Operational Amplifier | (4) |
| b) Discuss differentiator circuit using Op-amp | (10) |
| 14 a) Draw the circuit of an Integrator using Op-Amp and explain wave waveforms | (7) |
| b) Design an Inverting amplifier of gain 10 | (7) |

Module 3

- 15 a) Explain with circuit diagram, the operation of VCO (7)
b) Explain the working of Monostable multivibrator using IC 555 (7)
- 16 a) Define: 1) Pass band (4)
2) Cut off frequency
b) Explain about all types of active Active filter circuits (10)

Module 4

- 17 a) Implement the function $F(a,b,c)=\sum m (0,1,3,5,7)$ using 8:1 MUX (8)
b) Design De multiplexer circuit using logic gates (6)
- 18 a) Design a Full Adder circuit using NAND gate (10)
b) State and prove De Morgan's Theorems (4)

Module 5

- 19 Design a 3 bit synchronous down counter using JK FF (14)
- 20 Design a Mod -5 synchronous counter using T FF (14)
