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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Regular and Supplementary Examination December 2022 (2019 Scheme)

Course Code: ECT203

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1	Convert the decimal number 215 to following codes (i)BCD code (ii)Excess 3 code (iii) Gray code	(3)
2	Convert the decimal number 18.6875 into binary and hexadecimal.	(3)
3	Write Verilog Code for a XOR gate	(3)
4	Express f(A,B,C) = AB + AC' + BC in standard SOP form.	(3)
5	Design a 1-bit comparator circuit using logic gates.	(3)
6	Realize an 8:1 multiplexer using 4:1 multiplexers and gates.	(3)
7	Convert a JK flip-flop to D flip-flop.	(3)
8	Realize D latch using gates and write the Verilog code.	(3)
9	Define the following in terms of Logical families i) Propagation delay ii) fan out iii) Noise margin	(3)
10	Draw the circuit diagram of a CMOS- NOT gate and explain the working with truth table.	(3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11	a) Find the sum of two hexadecimal numbers $(85C)_{16}$ and $(23C6)_{16}$	(2)
	b) Covert each decimal number to binary and perform the subtraction **21.5_{10} $--13.25_{10}$** using (i)1's complement method(ii)2's complement method	(4)
	c) Explain the main differences between the Verilog terms (i)Wire and Reg (ii)Task and Function	(8)

12 a) How is the Hamming code word generated? The message "1001001" is coded in 7-bit even parity Hamming code, which is transmitted through a noisy channel. Decode the message, assuming that at most a single error occurred in each code word. (8)

b) Explain Verilog operators with examples. (6)

Module 2

13 a) Simplify the Boolean expression F (A, B, C, D) =∑m (0, 1, 2, 6, 8, 9, 10, 11) + d (3, 7, 14, 15) using K-Map and implement the simplified expression using universal gates. (8)

b) Prove the following Boolean rules

i. A+AB=A (6)

ii. A+A′B=A+B

14 a) Reduce the following function using Karnaugh map technique (8)

f (A, B, C, D) = πM (0, 2, 4, 10, 11, 14, 15) and implement the simplified expression using NAND gates.

b) Explain the significance of duality principle in Boolean algebra (6)

Module 3

15 a) Implement the following functions using MUX (9)

(i)AND

(ii)XOR (5)

iii) $f(A, B, C) = \sum m\ (0, 3, 5, 6)$

b) Write a verilog code to implement 4:1 multiplexer.

16 a) Implement a Full adder circuit using (9)

(i) 3: 8 decoder (ii) 1:8 demultiplexer (5)

b) Write a Verilog description for a one-bit full adder circuit

Module 4

17 a) Design a 3-bit synchronous up counter using T flip-flop. (9)

b) Explain the operation of a 4-bit Ring counter. (5)

18 a) Design a divide by 2N circuit using N number of flip-flops. Draw the truth table and waveforms. (7)

b) What is a race around condition related to JK Flip Flop? Explain how to eliminate the problem. (7)

Module 5

19 a) Describe the working of a 2-bit TTL NAND gate with Totem pole configuration. (8)

b) Explain the working of a transistor level CMOS NOR gate. (6)

20 a) Describe the working of a tristate TTL inverter (8)

b) Explain the working of a transistor level CMOS NAND gate. (6)

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