Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree (S,FE) Examination December 2022 (2015 scheme)

Course Code: EC207

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks.

Marks

1 a) Convert $(45.75)_{10}$ to Binary, Hexadecimal form and Octal form. (6)

b) Obtain the minimal sum of product of the following expression ABCD+AB'C'D'+AB'C+AB (9)

2 a) Perform the following operations (8)

(i) $(56)_{10} - (48)_{10}$ using 2's and 1's complement method

(ii) Represent $(478)_{10}$ in BCD and Excess-3 codes.

b) Design the circuit of a 3-line to 8-line decoder using basic gates (7)

3 a) What is Hamming code? Determine the Hamming code for the information 1001, with even parity. (7)

b) Design a magnitude comparator to compare two 2-bit numbers A = A1A0 and B = B1B0 (8)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Define the terms noise margin, propagation delay and power dissipation of logic families. Compare TTL and CMOS logic families showing the values of above-mentioned terms. (7)

b) Realize the following: i) T flip-flop using SR flip-flop ii) JK flip-flop using D flip-flop. (8)

5 a) Draw the circuit diagram of a transistor level CMOS NAND gate and explain the working with a truth table. (7)

b) Explain the working of a master slave JK flipflop, with the help of circuit diagram. (8)

6 a) Implement the following functions using PLA. (8)

$$F_1 = \sum_m (3,5,7)$$

$$F_2 = \sum_m (4,5,7)$$

b) Explain a MOD 6 asynchronous counter using J K Flip Flop. (7)

PART C

Answer any two full questions, each carries20 marks.

7 a) Draw the logic diagram of a four-bit, bi-directional serial in serial out (SISO) shift register with mode control and explain the working with timing diagram. (10)

b) Draw the state diagram for Moore and Mealy serial binary adder. (10)

8 a) Draw the logic diagram of a four-bit Johnson counter and explain the working with truth table and timing diagram. (10)

b) Reduce the following state table using implication chart technique. (10)

Present State	*Next State, z*	
	X=0	*X=1*
A	*A,0*	*B,0*
B	*D,0*	*C,1*
C	*F,0*	*E,0*
D	*D,0*	*F,0*
E	*B,0*	*G,0*
F	*G,0*	*C,1*
G	*A,0*	*F,0*

9 a) Draw the state diagram, transition table, D flip flop excitation table and state equation for the given state table. (10)

Present state	Next state		Output (Z)	
	X=0	X=1	X=0	X=1
A(00)	A	B	0	0
B(01)	C	B	0	0
C(10)	A	D	0	0
D(11)	C	B	1	0

b) Draw the logic diagram of a 4-bit ring counter and explain the working with timing diagram. (10)

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