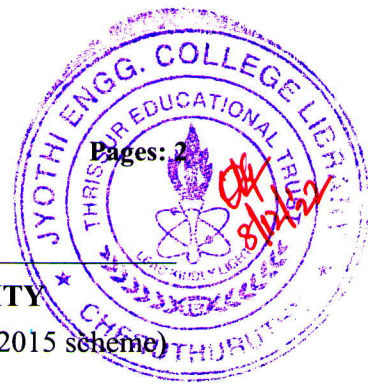C **08000CS203122005**

Reg No.:_____   Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
Third Semester B.Tech Degree (S,FE) Examination December 2022 (2015 scheme)

Course Code: CS203

Course Name: SWITCHING THEORY AND LOGIC DESIGN

Max. Marks: 100   Duration: 3 Hours

PART A
Answer all questions, each carries 3 marks.

Marks

1	Convert the following numbers to binary.	(3)

   a) $(326)_{10}$ b) $(23A)_{16}$ c) $(635)_8$

2 Find the 2's complement of the following.   (3)

   a) 1011010   b) 1010001

3 Simplify the following boolean functions to minimum number of literals.   (3)

   a) $x'y'z+x'yz+xy'z+xyz$ b) $x+x'y$

4 Convert the following function.   (3)

   a) $F_1=xy'+yz$ in sum of minterms.

   b) $F_2=(x+y)(y'+z)$ in product of maxterms.

PART B
Answer any two full questions, each carries 9 marks.

5 a) Perform the following BCD operation.   (4)

   i) BCD addition on decimal numbers 582 and 687.

   ii)BCD subtraction using 9's complement on 011110010010 and 100000010110.

   b) Perform 1's complement and 2's complement subtraction on the following.   (5)

   i) $(278)_{10}-(172)_{10}$ ii) $(0110101)_2-(0100110)_2$

6 Using   tabulation   method   simplify   the   Boolean   function   (9)
   $F(w,x,y,z)=\sum(2,3,4,6,,7,11,12,13,14)$ which has don't care conditions D(1,5,15).

7 a) Represent the decimal number 126.125 in IEEE 754 floating point single precision   (4)
      format.

   b) Using K-map simplify the Boolean function F as Sum of Products using the   (5)
      don't care conditions d.

      $F(w,x,y,z)=w'(x'y+xyz)+x(wy+wy'z)$

      $d(w,x,y,z)=x'y'z'+wz'(xy'+x'y)+w'xyz'$

PART C

Answer all questions, each carries 3 marks.

8   Implement exclusive-or operation using NAND gates only.   (3)

9   Differentiate full adder and half adder. Implement a full adder using two half   (3)
      adders.

10   What is an excitation table? Draw the truth table and the excitation table for JK   (3)
      flip flop.

11   Convert a D flip flop to JK flip flop.   (3)

PART D

Answer any two full questions, each carries 9 marks.

12   Design a combinational circuit whose input is a 4 bit number and output is the 2's   (9)
      complement of the input number.

13   a)   Explain race around condition. Explain the working of master slave flip flop with   (6)
        timing diagram.

     b)   Explain edge triggering and level triggering.   (3)

14   a)   Explain full adder. Implement a 4 bit ripple carry adder.   (5)

     b)   Explain a state table and state diagram with an example.   (4)

PART E

Answer any four full questions, each carries 10 marks.

15   Design a BCD ripple counter and explain its working with the help of the timing   (10)
      diagram.

16   Design a 4 bit universal shift register and explain its working.   (10)

17   Design a synchronous counter that counts the repeated sequence   (10)
      0,2,4,6,8,10,1,2,14 using T flip flop.

18   Explain Programmable logic array(PLA). Implement the following Boolean   (10)
      functions using a $3 \times 4 \times 2$ PLA.

      $F_1 (A, B, C) = (3, 5, 6, 7)$ and $F_2 (A, B, C) = (0, 2, 4, 7)$

19   a)   What is ROM? Explain various types of ROMS.   (5)

     b)   Write a HDL code for full adder in Structural model.   (5)

20   Draw and explain the flowchart for floating point addition and subtraction.   (10)

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