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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Seventh Semester B.Tech Degree Supplementary Examination June 2022 (2015 Scheme)

Course Code: CS405

Course Name: Computer System Architecture

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks. Marks

1 Explain with examples (i) flow dependence (ii) antidependence (4)

2 With a neat sketch give the details of data path architecture and control unit of a scalar processor. (4)

3 Distinguish between multiprocessor and multicomputers. (4)

4 Describe a generalized multiprocessor system with a neat diagram. (4)

5 Explain hierarchical bus system. (4)

6 Describe worm hole routing. (4)

7 How internal data forwarding is done among multiple functional unit? (4)

8 Write short notes on CDC score boarding. (4)

9 Elucidate the 4 states of context cycles. (4)

10 What do you understand by data flow graphs? Explain with an example. (4)

PART B

Answer any two full questions, each carries 9 marks.

11 a) Compare implicit parallelism and explicit parallelism. (3)

b) Consider the execution of an object code with $2x10^6$ instructions on a 400-MHz processor.The program consists of four major types of instructions .The instruction mix and number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment. (6)

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	60%
Load/store with cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

(i) Calculate the average CPI when the program is executed on a uniprocessor with the above trace results.

(ii) Calculate the corresponding MIPS rate based on obtained CPI

12 a) Differentiate CISC and RISC architecture. (5)

b) Explain VLIW architecture with a neat diagram. (4)

13 a) Define (i) MIPS rate (3)

(ii)Throughput rate

b) You are asked to perform capacity planning for a two-level memory system. The first level,M1,is a cache with three capacity choices of 64 Kbytes,128 Kbytes and 256 Kbytes.The second level, M2, is a main memory with a 4-byte capacity. (6)
Let c1 and c2 be the costs per byte and t1 and t2 the access times for M1 and M2 respectively. Assume c1 = 20c2 and t2 =10t1.The cache hit ratios for the three capacities are assumed to be 0.7,0.9 and 0.98,respectively.

(i) What is the average access time t_d in terms of t1=20 ns in the three cache designs?(Note that t1 is the time from CPU to M1 and t2 that from CPU to M2,not from M1 to M2).

(ii) Express the average byte cost of entire memory hierarchy if c2=$0.2/Kbyte.

PART C

Answer any two full questions, each carries 9 marks.

14 a) With a neat sketch discuss on multiport memory. (3)

b) (i) Draw a 16 input Omega network using 2x2 switches as building blocks. (6)
(ii) Show the switch settings for routing a message from node 1011 to node 0101 and from node 0111 too node 1001 simultaneously. Does blocking exist in this case?

15 a) Illustrate the flow control methods for resolving collisions between packets requesting the same outgoing channel. (6)

b) Discuss store and forward routing. (3)

16 a) Explain snoopy bus protocol. (3)

b) Consider the following reservation table for a four stage pipeline with a clock cycle τ=20ns.

	1	2	3	4	5	6
S1	x					x
S2		x		x		
S3			x			
S4				x	x	

(6)

(a) What are the forbidden latencies and the initial collision vector?
(b) Draw the state transition diagram for scheduling the pipeline.
(c) Determine the MAL associated with the shortest greedy cycle.
(d) Determine the pipeline throughput corresponding to the MAL and given T.

PART D

Answer any two full questions, each carries 12 marks.

17 a) Discuss the mechanisms for improving instruction pipelining. (6)

b) Explain different context switching policies. (6)

18 a) Implement the pipeline design for multiplication of two 8 bit integers. (12)

19 a) Describe various latency hiding techniques. (8)

b) Explain multithreading solution to asynchrony problem (4)

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