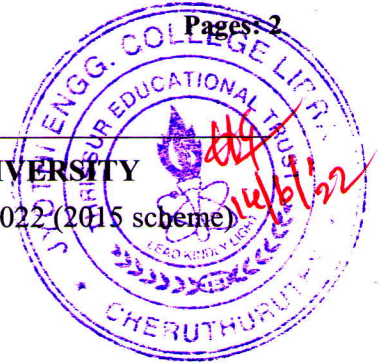


Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree (S,FE) Examination June 2022 (2015 scheme)

**Course Code: EE204****Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer all questions, each carries 5 marks*

Marks

- | | | |
|---|---|---|
| 1 | Do the following conversions,
i) $A5FD_{16}$ to Octal, ii) 257.56_{10} to binary, iii) 100101101_2 to Gray | 5 |
| 2 | State De Morgan's theorem and prove with truth table | 5 |
| 3 | Realise a full adder with two half adders with relevant equations and logic diagram. | 5 |
| 4 | Draw the logic circuit of a JK FF and explain its working with a truth table | 5 |
| 5 | Design a sequence generator with D-flip flop to generate a sequence of 8,4,2,1,8,4,2,1,..... | 5 |
| 6 | Differentiate between Mealy and Moore machines | 5 |
| 7 | Design a 3-bit flash type ADC and explain the working with logic circuit. | 5 |
| 8 | Write VHDL program of AND gate. | 5 |

PART B*Answer any two full questions, each carries 10 marks*

- | | | |
|----|---|----|
| 9 | What is the use of parity bit? Describe any one type of parity to generate and check a parity bit while sending a 4-bit binary number | 10 |
| 10 | Minimize the Boolean expression $f(A,B,C,D) = \prod M(0,2,4,8,10,12) + d(5,6,14)$ and implement using NAND- NAND logic | 10 |
| 11 | a) Draw and explain the working of a TTL NAND circuit | 6 |
| | b) Do the following operation by 2's complement method
$-36 + 25$ | 4 |

PART C*Answer any two full questions, each carries 10 marks*

- | | | |
|----|--|----|
| 12 | What is the need of carry look ahead adder? Explain with a two bit adder how carry look ahead adder achieves its objective | 10 |
|----|--|----|

- 13 Draw a decade ripple up counter, Explain the logic diagram and time diagram. 10
- 14 a) Realise the function, $F = \sum(0,2,5,6)$ by 4x1 MUX. 5
- b) Illustrate the working of PISO shift register. 5

PART D

Answer any two full questions, each carries 10 marks

- 15 Design a synchronous counter to count from 0 to 4 and realise by using JK flip flop. 10
- 16 Explain with circuits diagrams 10
- i) Weighted resistor DAC, ii) PLA
- 17 a) Describe the state diagram and state table of a Mealy model with an example. 5
- b) Differentiate between ROM and EPROM 5
