Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Sixth Semester B.Tech Degree (S,FE) Examination May 2022 (2015 Scheme)

Course Code: EC304

Course Name: VLSI

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks Marks

1 a) With neat sketches explain Czochralski process of crystal growth. Comment on the quality of the crystals grown through this technique. (8)

b) Discuss the oxidation technique employed in growing gate oxide and field oxide in MOSFETs. Justify your choice (2)

c) A dry oxidation process designed to grow 120 nm of oxide on silicon wafers at 900°C. What is the time required to obtain this thickness? What is the time if steam can be used instead? (5)

($B/A = 2.63\text{x}10^{-6}$ µm/sec, $B = 1.11\ \text{x}10^{-6}$ µm^2/sec for dry oxidation and $B/A = 4.2\text{x}10^{-5}$ µm/sec, $B = 4.32\text{x}10^{-6}$ µm^2/sec for wet oxidation. Assume a fictitious initial thickness of 0.020 µm for dry oxidation.)

2 a) Compare two step thermal diffusion and ion implantation techniques with their relative merits and demerits. Draw the doping profiles in each case and explain with necessary modelling equations. (10)

b) Explain the technique of fabricating resistors and capacitors in integrated circuits. (5)

3 a) With sketches, explain the fabrication process flow for realizing a CMOS inverter in N-well technology. Draw the mask for each step assuming positive photo resist. (10)

b) Define the following terms in the context of photolithography and explain how these terms are related to the pattern which is transferred on to silicon. (5)

i) Resolution ii) Depth of focus iii) Contrast

PART B

Answer any two full questions, each carries 15 marks

4 a) Draw the DC transfer characteristics of CMOS inverter. Derive an expression for the switching threshold of the device and explain how the β ratios of the devices affects the transfer characteristics, (10)

b) What are the sources of static power dissipation in CMOS inverter? (2)

c) Realize the logic function in complementary CMOS logic. (3)

$Y = \overline{A + C(B + D)}$

5 a) Draw the schematic, stick diagram and layout of two input NOR gates. (10)

b) List the factors on which the delay of CMOS inverter depend? Discuss methods to reduce this delay. (5)

6 a) Comment on the use of level restorer in pass transistor logic? With a circuit diagram and explain the operation. (5)

b) Discuss transmission gate logic? State the advantages over pass transistor logic? (3)

c) Implement 2:1 mux using transmission gates. Implement 4:1 mux using three 2:1 muxs. Explain the operation of the circuit. (7)

PART C

Answer any two full questions, each carries 20 marks

7 a) Draw the circuit of 6T SRAM cell. Explain its read and write operations. Comment on the sizing constraints of the transistors. (10)

b) Design a 4x4 NAND ROM to store the data (5)

Address	0	1	2	3
Data	1010	1100	0100	1111

c) Design a PLA with outputs, the sum of the following minterms. (5)

F1= m1+m6, F2 = m5+m6+m7, F3= m3+m2+m4+m7

8 a) Draw and explain the architecture of CLB based FPGA. (10)

b) Design a 16-bit linear carry select adder. Mark the critical path and calculate its worst-case delay. (10)

9 a) Design a circuit to multiply two 4-bit binary numbers $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ (10)

b) Design a 32-bit carry bypass adder using 4-bit carry bypass technique. Mark the critical path and calculate its worst-case delay. (10)

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