

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
Third Semester B.Tech Degree Examination December 2021 (2019 scheme)



Course Code: ECT203

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100

Duration: 3 Hours

PART A*Answer all questions. Each question carries 3 marks*

- | | Marks |
|---|-------|
| 1 Convert $(231.45)_8$ to equivalent decimal and binary | (3) |
| 2 Give a brief description of keywords in Verilog | (3) |
| 3 _____ | (3) |
| Reduce the expression $F = \overline{AB} + \overline{A} + AB$ using De-Morgan's theorem | |
| 4 Write a Verilog code for implementing a NOR gate | (3) |
| 5 Explain the working of a multiplexer | (3) |
| 6 Write a Verilog code for half subtractor | (3) |
| 7 Convert a JK flipflop to T flipflop | (3) |
| 8 Write a Verilog code for implementing D flipflop | (3) |
| 9 Define noise-margin | (3) |
| 10 Define propagation delay and power dissipation | (3) |

PART B*Answer any one full question from each module. Each question carries 14 marks***Module 1**

- 11 (a) Perform the following operations (6)
 (i) $(A5C)_{16} + (8E4)_{16}$ (ii) $(175.6)_8 - (47.7)_8$
- (b) What is Hamming code? The message 1100110 is coded in 7-bit even parity Hamming code which is transmitted through a noisy channel. Decode the message assuming that a single error occurred in the codeword (8)
- 12 (a) Find 11001-10001 using 1's and 2's complement arithmetic (8)
 (b) Explain the operators in Verilog (6)

Module 2

- 13 (a) Obtain the canonical POS expression of $F(A,B,C) = (A + \overline{B})(B + C)(A + \overline{C})$ (5)
 (b) Simply the expression $Y = \prod M(0,1,4,5,6,8,9,12,13,14)$ using K-Map and implement the simplified expression using NOR logic. (9)

- 14 For the logical expression $F = \bar{A} + AB + AB\bar{D} + A\bar{B}\bar{D} + C$ (14)
- (i) Obtain Canonical SOP expression
- (ii) Simplify the expression using K-Map
- (iii) Write Verilog code for the simplified expression

Module 3

- 15 (a) Design a full adder circuit (8)
- (b) Write a Verilog code for 1:4 demultiplexer (6)
- 16 (a) Implement the logic function $f(A,B,C) = \sum m(0,2,3,5)$ using (8)
- (i) 8:1 MUX (ii) 4:1 MUX
- (b) Design an octal to binary encoder (6)

Module 4

- 17 (a) Explain the operation of a JK flip-flop using NAND gates (6)
- (b) Explain the operation of a 4-bit Johnson counter with truth table and waveforms (8)
- 18 (a) Design a mod-6 synchronous up-counter using JK flip-flop (7)
- (b) Explain a PISO shift register using \overline{LOAD} /SHIFT (7)

Module 5

- 19 (a) Compare TTL & CMOS logic families in terms of fan-in, fan-out, supply voltage, propagation delay and noise margin (5)
- (b) Draw the circuit and explain the operation of transistor level TTL NAND gate (9)
- 20 (a) Draw the circuit diagram of a transistor level TTL Inverter and explain the working (5)
- (b) Draw the circuit and explain the operation of transistor level CMOS NAND gate (9)
