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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Fourth Semester B.Tech Degree (S,FE) Examination August 2021 (2015 Scheme)

Course Code: CS202

Course Name: COMPUTER ORGANISATION AND ARCHITECTURE (CS, IT) Max, Marks: 100 Duration: 3 Hours

PART A Answer all questions, each carries 3 marks

1		How are nested subroutine calls internally implemented in a computer?	3
2		Index addressing mode is useful in dealing with lists and arrays. Justify the	3
		statement.	
3		List the control signals that are activated while storing a word in memory using a	3
		single bus organization	
4		Design a 3×2 array multiplier	3
		PART B	
		Answer any two questions, each carries 9 marks	
5	a)	Write notes on one address, two address and three address instructions with proper	5
		examples.	
	b)	List and explain any 4 addressing modes with examples	4
•6	a)	Write a program that can evaluate the expression $A \times B + C \times D$ in a single	5
		accumulator processor. Assume that the processor has Load, Store, Multiply and	
		Add instructions, and that all values fit in the accumulator.	
	b)	Divide 24 by 7 using restoring division algorithm	4
7	a)	Draw and explain the flowchart of floating point multiplication algorithm	5
	b)	Explain multiple bus organization with the help of a diagram	4
		PART C	
		Answer all question, each carries 3 marks	
8		List the functions of I/O interface circuits.	3
9		Illustrate how various devices are addressed on the USB?	3
10		What is MFC signal? How is it related to memory access time?	3
11		With a neat diagram explain the structure of a synchronous DRAM	3

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PART D

a)	Answer any two questions, each carries 9 marks How program controlled I/O is performed using polling?	5			
b)	Explain the working of a PCI bus with the help of timing diagrams.	4			
a)	Explain internal organization of memory chips with the help of a neat diagram.	5			
b)	Explain direct cache mapping with the help of an example. What are the issues	4			
	associated with direct mapping?				
a)	Illustrate USB architecture and working with the help of a neat diagram.	5			
b)	Write notes on flash memory. List its advantages and disadvantages	4			
PART E					
	Answer any four questions, each carries 10 marks				
a)	Draw the block diagram of the hardware that implements the following register	5			
	transfer statement:				
	$yT_2: R_2 \leftarrow R_1, R_1 \leftarrow R_2$				
b)	List and discuss about shift and logic microoperations.	5			
	Explain how control signals are generated using PLA control, using an example	10			
	with a neat diagram				
	Describe the basic organization of a microprogrammed CPU with the help of a	10			
	diagram				
	List and explain the different control organisations with the help of neat diagrams	10			
a)	Starting from an initial value of $R=11011101$, determine the sequence of binary	5			
	values in R after a logical shift-left, followed by a circular shift-right, followed by				
	a logical shift-right and a circular shift left.				
b)	Write notes on status register.	5			
	 b) a) b) a) b) a) b) 	 a) How program controlled I/O is performed using polling? b) Explain the working of a PCI bus with the help of timing diagrams. a) Explain internal organization of memory chips with the help of a neat diagram. b) Explain direct cache mapping with the help of an example. What are the issues associated with direct mapping? a) Illustrate USB architecture and working with the help of a neat diagram. b) Write notes on flash memory. List its advantages and disadvantages PART E Answer any four questions, each carries 10 marks a) Draw the block diagram of the hardware that implements the following register transfer statement: yT₂: R₂ ← R₁, R₁ ← R₂ b) List and discuss about shift and logic microoperations. Explain how control signals are generated using PLA control, using an example with a neat diagram Describe the basic organization of a microprogrammed CPU with the help of a diagram List and explain the different control organisations with the help of neat diagramss a) Starting from an initial value of R=11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift left.			

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