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APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Seventh Semester B.Tech Degree Supplementary Examination August 2021

COLLEGE OF ENGG. THRISSUR EDUCATIONAL TRUST CHERUTHURUTHY

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks. Marks

1		With neat sketch explain flynn's classification of computer architecture.	(4)
2		Discuss pipelining in superscalar processors.	(4)
3		Explain shared local memories model and hierarchical cluster model of NUMA multiprocessor system.	(4)
4		With the help of diagram explain interconnection structures in a generalized multiprocessor system	(4)
5		List any three causes of cache inconsistency. Explain any one in detail.	(4)
6		Write a short note on flow control strategies for resolving collision between 2 packets.	(4)
7		Explain the importance of Tomasulo's algorithm for dynamic instruction scheduling.	(4)
8		List and explain the possible hazards that can occur between read and write operations in an instruction pipeline?	(4)
9		Explain the four context switching polices for multithreaded architecture.	(4)
10		Write a short note on distributed caching.	(4)

PART B

Answer any two full questions, each carries 9 marks.

11	a)	Consider 2 programs A & B that solves a given problem. A is scheduled to run on a processor P1 operating at 1 GHz and B is scheduled to run on processor P2 running at 1.4 GHz. A has total 10000 instructions out of that 20% are branch instructions, 40% load and store and rest are ALU instructions. B is composed of 25% branch instructions. The number of load and store instructions in B is twice the count of ALU instructions. Total instruction count of B is 12000. In both P1 and P2 branch instructions have an average CPI of 5 and ALU instructions have an average CPI of 1.5. Both architectures differ in CPI for the	(6)

load and store instructions, which are 2 and 3 for P1 and P2 respectively. Find out which mapping solves (A on P1 or B on P2) the problem faster and how much?

b) Define the following terms, (3)

1. Flow dependence 2. Anidependence 3. Output dependence

12 a) Compare the characteristics of typical RISC and CISC architectures. (6)

b) Explain the inclusion, coherence and locality of reference properties of memory hierarchy. (3)

13 a) Suppose that we want to enhance the floating point operations of a processor by introducing a new advanced floating point unit. Let the new floating point unit is 10 times faster on floating point computations than original processor. Assume a program has 40% floating point operations. What is the overall speedup gained by incorporating the enhancement? (4)

b) With a neat diagram, explain about VLIW architecture. (5)

PART C

Answer any two full questions, each carries 9 marks.

14 a) Describe how multiport memories used in a multistage network. (3)

b) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutation $\pi 1 = (0,5,3,7,1)(2,6),(4)$. Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context. (6)

15 a) Consider the five-stage pipelined processor specified by the following reservation table and answer the following: (S indicate the stages) (6)

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

1. List the set of forbidden latencies and the collision vector.
2. Draw the state transition diagram showing all possible initial sequences without causing a collision in the pipeline.
3. List all the simple and greedy cycles from the state diagram.
4. Determine the minimal average latency (MAL).

b) Consider a 16-node hypercube network. Based on the E-cube routing algorithm, show how to route a message from node (0110) to node (1101). All intermediate nodes must be identified on the routing path. (3)

16 a) With a neat figure, explain about full mapped directory based protocol. (4)

b) Explain about Store-and Forward and Wormhole routing schemes with diagram. Analyse and compare the communication latencies. (5)

PART D

Answer any two full questions, each carries 12 marks.

17 a) List and explain mechanisms for improving the performance of instruction pipelining. (9)

b) Explain the effect of branching in instruction pipelining. (3)

18 a) List the latency hiding techniques used in distributed shared memory multi computers. Explain any two in detail. (7)

b) Explain the MIT/Motorola *T prototype architecture. (5)

19 a) How Carry Save adder (CSA) and Carry propagate adder (CPA) can be used in a fixed point multiplication pipeline unit? (4)

b) Write a short note on fine-grain parallelism. (4)

c) Differentiate between static and dynamic data flow computers. (4)

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