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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Sixth Semester B.Tech Degree Regular and Supplementary Examination July 2021

Course Code: AE306

Course Name: DIGITAL SIGNAL PROCESSING

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks. Marks

1 a) Find the 8 point DFT of the sequence x(n) = [1, -1,-1,-1,1,1,1,-1] using DIT FFT algorithm. (7)

b) What is an antialiasing filter? How do you prevent aliasing while sampling a CT signal? (5)

c) Prove that DFT [x ((n-m)) $_N$] = $e^{-j2\pi km/N}$ x(k). (3)

2 a) State any 5 properties of ROC of Z transform. (5)

b) Determine the Z transform and ROC of the signal x(n)= -b^n u(-n-1) (5)

c) Find the nyquist rate of x(t)=sin 400πt+cos2500πt (5)

3 a) Find the inverse Z transform of X(Z) = $\frac{Z(Z^2-4Z+5)}{(Z-3)(Z-1)(Z-2)}$ for ROC i) 2< |Z|<3 ii) |Z|>3 (10)

b) Compute 4 point IDFT of the sequence Y(k)= {1,0,1,0} (5)

PART B

Answer any two full questions, each carries 15 marks.

4 a) For the given specification design an analog Butterworth filter 0.9 ≤ |H (jΩ)| ≤ 1 for 0 ≤ Ω ≤ 0.2π. |H(jΩ)| ≤ 0.2 for 0.4π ≤ Ω ≤ π. (9)

b) Explain the frequency transformation in the analog domain. (6)

5 a) Using the bilinear transform, design a high pass filter, monotonic in passband with cut-off frequency of 1000 Hz and down 10dB at 350 Hz. The sampling frequency is 5000 Hz. (9)

b) With the frequency response explain the general properties of a typical window for filter design. (6)

6 a) Design an ideal low pass filter with a frequency response (10)

$H_d(e^{jw}) = 1$ for $-\pi/2 \leq w \leq \pi/2$

$= 0$ for $\pi/2 \leq |w| \leq \pi$ find the value of h(n).N=11, Find the transfer function of the filter.

b) Explain Gibbs phenomenon. (5)

PART C

Answer any two full questions, each carries 20 marks.

7 a) Obtain the direct form I, direct form II, cascade and parallel realization of the system $y(n) = -0.1y(n-1) + 0.2y(n-2) + 3x(n) + 3.6x(n-1) + 0.6x(n-2)$ (10)

b) Draw and explain the architecture of TMS 320C 54X. (10)

8 a) Explain different forms of fixed point number representation in DSP. (5)

b) Explain errors due to truncation and rounding. (6)

c) Explain the Von-Neumann and Harvard architecture with a neat block diagram. (9)

9 a) Explain (12)

I. Multiply Accumulate Unit

II. Pipelining

b) Explain the effects of input quantization error. (8)

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