APJ ABDULKALAM TECHNOLOGICAL UNIVERSITY

08 PALAKKAD CLUSTER

Name: .....

Q. P. Code : CESP0820141-I (Pages: 2) Reg. No:.....

FIRST SEMESTER M.TECH. DEGREE EXAMINATION MARCH 2021

Branch: Electronics & Communication Engineering **Specialization: Communication Engineering & Signal Processing**

08EC6241 / 08EC6541 Design of Digital Signal Processing Systems

(Common to CESP and ECE)

Time: 2 hour 15 minutes **Max. Marks: 60**

Answer all six questions.

Modules 1 to 6: Part 'a' of each question is compulsory and answer either part 'b' or part 'c' of each question.

Module 1

Q. No.		Marks
1.a	Explain execute packets in DSP system	3
	Answer b or c	
b	Explain the interrupts system of TMS320C6713 DSP Processors	6
c	With a neat block diagram explain TMS320C6713 architecture	6

Module 2

Q. No.		Marks
2. a	Describe the addressing modes in TMS 320C6713 DSP processor	3
	Answer b or c	
b	Write a c program with callable assembly function to find the sum of products in an array	6
c	With suitable examples explain various types of instructions used in TMS320C6x DSP Processors	6

Module 3

Q. No.		Marks
3.a	What are the different ways to invoking assembly language in C-code	3
	Answer b or c	
b	Explain briefly about compiler and assembler	6

c	Illustrate the block diagram of AIC23 stereo codec	6

Q. No.	Module 4	Marks
4.a	Enumerate the features of adaptive filters	3
	Answer b or c	
b	Using MATLAB, write a program to compute the DFT of the 8-point sequence x(n)={1,1,1,1,0,0,0,0}. Also compute the IDFT of the 8 DFT coefficients to verify the DFT results.	6
c	Design a butterworth HPF using MATLAB with passband and stop band attenuations 0.3 and 20 dB at passband and stopband frequencies of 500 Hz and 900 Hz respectively. Sampling frequency is 2.5 kHz	6

Q. No.	Module 5	Marks
5.a	Explain the finite word length effects in the implementation of FFT algorithms	4
	Answer b or c	
b	Explain the implementation filters using DSP systems	8
c	Explain the DTMF generation algorithm	8

Q. No.	Module 6	Marks
6.a	Explain the significance of DSP controllers	4
	Answer b or c	
b	With a help of block diagram explain how a PLL is implemented using DSP system	8
c	With a help of block diagram explain how a FSK system is implemented using DSP system	8