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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Examination December 2020 (2019 Scheme)

Course Code: ECT203

Course Name: LOGIC CIRCUIT DESIGN

Max. Marks: 100 **Duration: 3 Hours**

PART A

Answer all questions. Each question carries 3 marks Marks

1	Convert $(3A9E.B)_{16}$ to binary and decimal.	(3)
2	Convert $(25)_{10}$ to binary, gray and BCD.	(3)
3	Express the boolean function $F(A,B,C) = A + \bar{B}C$ as sum of minterms.	(3)
4	Write Verilog Code for a NAND gate.	(3)
5	Implement a 4-input binary decoder using basic gates.	(3)
6	Explain the working of a 4-bit parallel adder.	(3)
7	Obtain the excitation table and characteristic equation of a T flip-flop.	(3)
8	Convert a JK flip-flop to D flip-flop.	(3)
9	Distinguish between fan-in and fan-out.	(3)
10	Explain noise margin.	(3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11	(a) Subtract 27 from 75 using 2's and 1's complement arithmetic	(8)
	(b) Explain fixed and floating point representation of numbers	(6)
12	(a) What is Hamming code? How is the Hamming codeword generated? Encode the data bits 1011 into 7-bit even Hamming code.	(8)
	(b) Give a brief description of identifiers and keywords in Verilog	(6)

Module 2

13	(a) Implement an EX-OR gate using universal gates	(6)
	(b) Simplify the Boolean expression $F(A,B,C,D) = \Sigma m(1,3,10)+d(0,2,8,12)$ using K-Map and implement the simplified expression using universal gates.	(8)

14	(a) Reduce the Boolean expression F=∏M(1,2,3,4,10,11,15) using K-Map	(7)
	(b) Write Verilog code for implementing the above function	(7)

Module 3

15	(a) Design a BCD adder circuit.	(8)
	(b) Write Verilog code for full subtractor circuit.	(6)
16	(a) Design a 3-bit magnitude comparator.	(8)
	(b) Implement the logic function F(A,B,C,D)= Σ m(1,3,4,11,12,13,14,15) using 8 : 1 MUX	(6)

Module 4

17	(a) Explain the operation of a 4-bit Johnson counter with truth table and waveforms.	(7)
	(b) Design a mod-10 asynchronous counter using T flip-flop.	(7)
18	Design a mod -16 synchronous counter using JK flip-flop.	(14)

Module 5

19	(a) Explain the working of a transistor level TTL NAND gate.	(8)
	(b) Draw and explain the working of a transistor level CMOS inverter.	(6)
20	(a) Explain the working of a transistor level CMOS NOR gate.	(8)
	(b) Compare TTL & CMOS logic families in terms of fan-in, fan-out, supply voltage, power supply and propagation delay and power dissipation.	(6)

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