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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Third Semester B.Tech Degree Examination December 2020 (2019 Scheme)

Course Code: MRT203
Course Name: ANALOG AND DIGITAL ELECTRONICS

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions. Each question carries 3 marks Marks

1	Differentiate between amplifier and oscillator.	(3)
2	Briefly explain the concept of feedback.	(3)
3	With neat sketch explain the frequency response of op-amp.	(3)
4	Discuss with waveform how op-amp operates as a comparator in inverting mode.	(3)
5	Write a short note on wide band pass filter with neat circuit diagram.	(3)
6	Summarize the following a) Lock range b) Capture range.	(3)
7	Design a Half Adder circuit and explain briefly.	(3)
8	Using K-map simplify the Boolean expression Y= $A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$	(3)
9	Distinguish between synchronous and asynchronous circuits.	(3)
10	Explain the D flip flop with logic circuit and truth table.	(3)

PART B

Answer any one full question from each module. Each question carries 14 marks

Module 1

11	a)	Derive an expression for the frequency of Hartley Oscillator and explain briefly.	(6)
	b)	Elaborate in detail about class B push pull amplifier with a neat circuit diagram and find out the efficiency.	(8)

12	a)	Describe how N-channel JFET is constructed. Explain how pinch off occurs in JFET.	(8)
	b)	What are the advantages of the FET and BJT?	(6)

Module 2

13	a)	Discuss about various methods to convert Voltage to current (V to I) using Op-Amp.	(5)
	b)	Illustrate the following (i) Sample and Hold (S/H) circuit (ii) Inverting Comparator (iii) Non Inverting Comparator	(9)
14	a)	Show that how we can use op-amp for integration.	(5)
	b)	With suitable diagrams explain in detail about regenerative comparator.	(9)

Module 3

15		With suitable diagram explain IC 555 Timer as an Astable multivibrator.	(14)
16	a)	Derive the expression for the gain for a first order active LPF. Sketch the frequency response plot.	(9)
	b)	Explain the block schematic of PLL.	(5)

Module 4

17	a)	State and prove Demorgan's theorem.	(4)
	b)	Explain the working of an Octal to Binary (8 to 3) Encoder with a neat diagram and truth table.	(10)
18		Using Quine McCluskey method simplify $f(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$	(14)

Module 5

19		Design a sequence detector that produces an output "1" whenever the non-overlapping sequence 1101 is detected.	(14)
20	a)	Describe in detail about 4 bit Serial In Serial Out (SISO) shift register using negative edge triggered D Flip Flop.	(7)
	b)	Design an Asynchronous UP counter and explain using timing diagram and truth table	(7)

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