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Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Seventh Semester B.Tech Degree Examination (Regular and Supplementary), December 2020

Course Code: CS405

Course Name: COMPUTER SYSTEM ARCHITECTURE

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 4 marks. Marks

1		State Amdahl's law. Suppose that we want to enhance the processor used for a server machine. The new processor is 15 time faster on computation in the serving applications than the original processor. Assuming the original processor is busy with computation 30% and waiting for I/O 70% time, what is the overall speedup gained by incorporating the enhancement.	(4)
2		Explain UMA model for Multiprocessor Systems.	(4)
3		Define the inclusion property of a memory hierarchy with diagram.	(4)
4		How does cache inconsistency occur in caches due to sharing writable data and process migration?	(4)
5		Differentiate between synchronous and asynchronous model of linear pipeline processors.	(4)
6		Explain different flow control strategies for resolving a collision between two packets.	(4)
7		What is dynamic instruction scheduling?	(4)
8		What is meant by pipeline stalling?	(4)
9		Explain the different context switching policies adopted by multithreaded architectures.	(4)
10		Write short notes on fine-grain parallelism.	(4)

PART B

Answer any two full questions, each carries 9 marks.

11	a)	Explain different types of data dependence with example.	(4)

b) Consider the execution of an object code with 100,000 instructions on a 40-MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type are given below based on the result of a program trace experiment. (5)

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	60%
Floating point Arithmetic	2	20%
Load/store	4	10%
Memory reference	6	10%

Calculate the average CPI, MIPS rate and Execution time.

12 a) Compare CISC and RISC machines in terms of addressing modes, instruction format and CPI. (3)

b) Consider the design of a three-level memory hierarchy with the following specifications for memory characteristics: (6)

Memory Level	Access time	Capacity	Cost/Kbyte
Cache	t1 = 25 ns	S1 = 512 Kbytes	C1 = $0.12
Main memory	t2 = **unknown**	S2 = 32 Mbytes	C2 = $0.02
Disk array	t3 = 4 ms	S3 = **unknown**	C3 = $0.00002

Our aim is to achieve an effective memory-access time t=850 ns with a cache hit ratio h1 = 0.98 and a hit ratio h2 = 0.99 in the main memory. Also, the total cost is upper-bounded by $1,500. Calculate unknown specifications based on these conditions.

13 a) Explain Flynn's classification of computer architecture. (3)

b) Explain pipelining in following processors. (6)

i)Superscalar processor ii) VLIW processor iii) Vector processor

PART C

Answer any two full questions, each carries 9 marks.

14 a) Design an 8 input omega network using 2X2 switches as building blocks. Show the switch settings for the permutation $\pi 1=(0,5,4,7,2)(1,6)(3)$. Show the conflicts in switch settings, if any. Explain blocking and non-blocking networks in this context. (6)

b) Explain the significance of multiport memory. (3)

15 a) Explain Dimension order routing with example. (4)

b) Consider the following pipeline reservation table: (5)

	1	2	3	4	5	6
S1	X				X	
S2			X			
S3		X		X		X

i) What are the forbidden and permissible latencies?

ii) Draw the state transition diagram.

iii) List all the simple cycles and greedy cycles.

iv) Determine the minimal average latency (MAL).

16 a) Define Write –invalidate Snoopy Bus Protocol. Draw and explain the 2 state transition graphs for a cache block using write –invalidate write -through and write-back snoopy bus protocols. (6)

b) Compare the communication latencies of Store-and Forward and Wormhole routing schemes. (3)

PART D

Answer any two full questions, each carries 12 marks.

17 a) Describe the various mechanisms for instruction pipelining. (6)

b) Compare static and dynamic branch prediction strategies. Explain how delayed branches reduces branch penalty. (6)

18 a) Explain any three latency hiding techniques used in distributed shared memory multicomputers. (6)

b) What are the problems of asynchrony and their solutions in massively parallel processors? (6)

19 a) Explain the concept of in-order issue and out-of-order issue with respect to superscalar processor. (6)

b) Explain the data flow architecture. (6)

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