D 30333 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2008

EC 2K 305/AI 2K 305. DIGITAL ELECTRONICS

Time : Three Hours Maximum : 100 Marks

1. (a) Show that $F = A + B + \overline{C}$ can be implemented with one 2 input NAND gate and one 2 input NOR gate.

   (b) Show how EX-OR and EX-NOR gates can be used as inverters.

   (c) Convert a D-flip-flop to a JK flip-flop by including input gates to the D-flip-flop.

   (d) Show that a full subtractor can be constructed with two half subtractors and an OR gate.

   (e) What is the difference between a serial and parallel transfer ?

   (f) Construct a D-flip-flop with only four NAND gates.

   (g) What is meant by bipolar inverter ?

   (h) Define Propagation delay, Noise margin in logic gates.

   (8 × 5 = 40 marks)

2. (a) (i) Implement the following Boolean function with a 4 × 1 MUX and external gates. Connect A and B to selection lines. The input requirements for the four data lines will be a function of variables C and D.

$$F(A, B, C, D) = \Sigma (1, 3, 4, 11, 12, 13, 14, 15).$$

   (7 marks)

   (ii) An 8 × 1 MUX has inputs A, B and C connected to the selection lines S_2, S_1 and S_0 respectively. The data inputs I_0 through I_7 are as follows :

$$I_1 = I_2 = I_7 = 0, I_3 = I_5 = 1, I_0 = I_4 = D, I_6 = \overline{D}.$$

   Determine the Boolean function that the multiplier implements.

   (8 marks)

Or

   (b) Design a code converter that converts a decimal digit from 84-2-1 code to BCD. (15 marks)

3. (a) Draw the logic diagram of 4 bit adder subtractor and explain. (15 marks)

Or

   (b) Draw the block diagram of BCD adder and explain. (15 marks)

Turn over

4. (a) Design a sequential circuit with two JK flip-flops, A and B and two inputs E and X. If E = 0, the circuit remains in the same state regardless of the value of X. When E = 1 and X = 1, it goes through the state transitions from 00 to 01 to 10 to 11 back to 00 and repeats. When E = 1 and X = 0 the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00 and repeats.

(15 marks)

Or

(b) Design a synchronous counter which counts

0, 1, 3, 6, 8, 11, 14, ... repeats.

Use JK flip-flops.

(15 marks)

5. (a) Draw the circuit of Schottky TTL and explain. (15 marks)

Or

(b) Write short notes on the following :—

(i) MOS inverter.

(ii) Rise time and fall time in CMOS gates.

(iii) Semiconductor memories.

(3 × 5 = 15 marks)

[4 × 15 = 60 marks]