C 27027 (2 Pages)

Name.....

Reg. No.....

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EIGHTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2003

CSE 805 (D)—COMPUTER ARCHITECTURE

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

1. (a) Distinguish among computer terminologies in each of the following groups :—

   (i) Control flow computer verus Data flow computers.

   (ii) Serial processing verus Parallel processing.

   (b) Compare temporal, spatial and sequential localities.

   (c) Explain S-access interleaved memory organisation.

   (d) Why is there a need to prefetch instructions in a pipelined unit ? Explain different ways of prefectching instructions.

   (e) Differentiate between simple cycle and greedy cycle with an example.

   (f) Explain the various fields of a vector instruction.

   (g) Explain the data routing mechanism of an SIMD computer.

   (h) What is the difference between cross cluster and intra cluster memory occurs in a multiprocessor system ?

(8 × 5 = 40 marks)

2. (a) (i) Explain different ways of achieving parallelism in a uniprocessor system. (8 marks)

   (ii) Give any *four* parallel processing application. (7 marks)

Or

   (b) (i) Give the classification of pipelines based on the configuration and control strategies. (7 marks)

   (ii) With a neat diagram, explain the pipelined multiplier built with a carry save-adder tree. (8 marks)

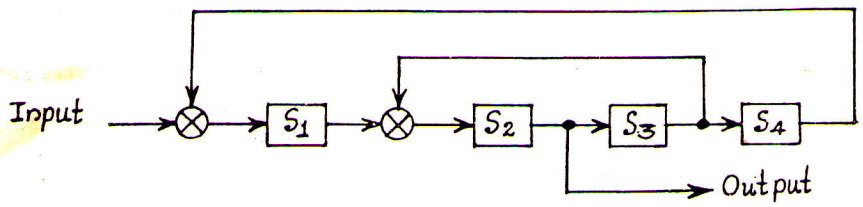
3. (a) (i) What are pipline hazards ? Give any one approach of resolving it. (8 marks)

   (ii) Explain different ways of enhancing the vector processing capabilities. (7 marks)

Or

Turn over

(b) (i) Consider a pipelined processor with four stages. All successor stages after each stage must be used in successive clock periods. The processor is shown in figure below.



Answer the following questions associated with the evaluation time of six pipeline clock periods.

(1) Write out the reservations table for this pipeline with six columns and four rows.

(2) List the set of forbidden latencies between task initiations.

(3) Draw the initial collision vector.

(4) Draw the state diagram which shows all the possible latency cycles.

(5) List all the simple cycles from the state diagram.

(6) List all the greed cycles.

(7) What is the value of the minimum average latency ?

(8) Indicate the minimum constant latency for this pipeline.

(9) What is the mammal throughput of this pipeline ?

(15 marks)

4. (a) (i) Explain the mesh connected Illiac Network. (8 marks)

(ii) Explain how matrix multiplication is performed in SIMD computer. (7 marks)

Or

(b) (i) Clearly specify the steps involved in performing merge sorting using M(5,4) sorting algorithm with an example.

(8 marks)

(ii) Explain the organisation and working of an associative memory. (7 marks)

5. (a) (i) What are the processor characteristics of a multiprocessor system ? (7 marks)

(ii) Explain the different types of multiprocessor operating systems. (8 marks)

Or

(b) (i) Explain any one partitioned matrix algorithm implemented using VLSI technology.

(7 marks)

(ii) In the following block of computations, a and b are two external inputs and 'z' is the final output. Two intermediate results are labelled x and y.

$$x \leftarrow a * a \; ; y \leftarrow b * b \; ; z \leftarrow (x + y) / (x - y)$$

(1) Draw the data flow graph for this code.

(2) Show that template implementation of the data flow graph in question (1) above.

(3) Indicate the events that can be done in parallel, in the execution of the above block of codes.

(8 marks)

(4 × 15 = 60 marks)