D 23460 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JANUARY 2003

CS2K/IT2K 305. SWITCHING THEORY AND LOGIC DESIGN

(New Scheme)

Time : Three Hours Maximum : 100 Marks

1. (a) (i) Find the 10's complement of $(935)_{11}$. (3 marks)

(ii) Convert the following numbers :—

(1) $(956.61)_{10}$ to BCD. (1 mark)

(2) $(110101110110)_2$ to hexadecimal. (1 mark)

(b) Explain Quine-McClausky algorithm with example. (5 marks)

(c) Design a two bit comparator circuit with basic gates. (5 marks)

(d) Differentiate Multiplexers and Demultiplexers. (5 marks)

(e) Prove that an experiment that detects all faults on the inputs of a network and on its reconverging paths detects all single faults within the network as well. (5 marks)

(f) Explain different types of ROM. (5 marks)

(g) What are the differences between counter and shift registers ? (5 marks)

(h) Explain the advantages of a master slave flip-flop over an edge triggered type in certain applications. (5 marks)

[8 × 5 = 40 marks]

2. (a) (i) Simplify the Boolean function F using the don't care condition d in sum of products and products of sums :

(1) $F = A'B'D' + A'CD + A'BC$
$d = A'BC'D + ACD + AB'D'$ (5 marks)

(2) $F = w'(x'y + x'y' + xyz) + \bar{x}z'(y + w)$
$d = w'x(y'z + yz') + xyz.$ (5 marks)

(ii) Prove that if $w'x + yz' = 0$ then $wx + y'(w' + z') = wx + xz + x'z' + w'y'z.$ (5 marks)

Or

(b) Use the QM procedure to generate the set of prime implicants and to obtain all minimal expressions for the following functions :—

(i) $f(w, x, y, z) = \Sigma(1, 5, 6, 12, 13, 14) + \Sigma_\phi(2, 4).$ (8 marks)

(ii) $f(w, x, y, z) = \Sigma(0, 1, 4, 5, 6, 7, 9, 11, 15) + \Sigma_\phi(10, 14).$ (7 marks)

Turn over

3. (a) (i) Design a 4-bit carry look-ahead adder circuit. (7 marks)

(ii) Explain the design of comparator circuit using 4-bit binary adder MSI circuit. (8 marks)

Or

(b) (i) Design an even parity generators and checkers. (7 marks)

(ii) A combinational circuit is defined by the following three functions :—

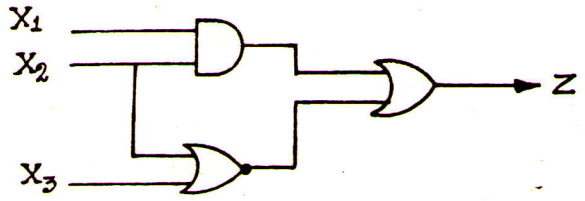
$F_1 = x'y' + xyz'$

$F_2 = x' + y$

$F_3 = xy + x'y'$

Design a circuit with a decoder and external gates. (8 marks)

4. (a) For the 3-input circuit



(i) Draw the table giving the set of all possible single fault and the faulty and fault free response. (7 marks)

(ii) With the help of the above table, construct the fault cover table and derive the minimum complete test set. (8 marks)

Or

(b) (i) Explain programmable logic array. (5 marks)

(ii) A combinational circuit is defined by the functions :

$F_1 (A, B, C) = \Sigma (3, 5, 6, 7)$

$F_2 (A, B, C) = \Sigma (0, 2, 4, 7)$

Implement the circuit with a PLA having three inputs, four product terms and two outputs. (10 marks)

5. (a) Develop a synchronous 3-bit up/down counter with a gray code sequence. The counter should count up or down depending on the value of the control input. (15 marks)

Or

(b) (i) Design a counter with the binary sequence 0, 1, 3, 2, 6, 4, 5, 7 and repeat. Use RS flip-flop.

(ii) Design and draw the circuit of a 3-bit up/down synchronous counter.

[4 × 15 = 60 marks]