D 23454 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JANUARY 2003

AI2K/EC2K 305. DIGITAL ELECTRONICS

(New Scheme)

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Assume suitable data that are not given.

1. (a) What are universal gates ? Show that EX-NOR function can be realized using only four numbers of NOR gates.

(b) Find the minimum sum-of-products expression for the function :

$$f(a, b, c, d) = \pi M(0, 2, 4, 6, 8) \cdot \underset{d}{\pi} M(1, 12, 9, 15).$$

(c) Design a 4 bit BCD adder using 4-bit binary address.

(d) What are state tables and state diagrams ? Explain.

(e) Explain with a logic diagram how a 4-bit JK flip-flop based serial-in-serial-out shift register be used to work as a 4-bit Johnson counter.

(f) What are finite state machine ? Explain the general model for a finite state machine.

(g) Draw the circuit configuration of a two input CMOS NAND gate and explain its operation.

(h) If the memory chip size is 8K × 8 :

(i) How many address lines are there in the single chip of memory ?

(ii) How many chips are required to make a 64K bytes of memory ?

(iii) How many address lines are needed for 64K bytes of memory.

(8 × 5 = 40 marks)

2. (a) Design a 4-bit gray to binary converter. Implement the circuit :

(i) Using only EX-OR gates.

(ii) Using only NAND gates.

Or

(b) For the expression :

$$G(A, B, C, D, E) = \Sigma m(0, 2, 6, 7, 8, 10, 11, 12, 13, 14, 16, 18, 19, 29, 30) + \Sigma m(4, 9, 21)$$

(i) Find the all the prime implicants.

(ii) Write down the minimum sum-of-product expression.

(iii) Also find if there were $n\theta$ don't care terms present in the original function how would your answer to be changed ?

(15 marks)

Turn over

3. (a) Design a 4-bit adder with look ahead carry. What are the advantages of this circuit over a 4-bit carry ripple adder ?

Or

(b) (i) Draw the logic diagram of a 4-bit shift register capable of performing following operation PIPO, SIPO and PISO.

(ii) Explain the use of shift registers.

(15 marks)

4. (a) Design a synchronous finite state machine which will sequence from state A = 00 to state B = 11 to state C = 10 to state D = 01, then reverse itself at state A and state D if the input X is high. Any time the X-input is low the circuit is to revert to state A and hold. Carry out all the steps for the design. You may use d-flip-flops in your design.

Or

(b) A long sequence of pulses enter the input of a synchronous sequential circuit which produces an output pulse $z = 1$ whenever the sequence 1101 occurs at the input (X). Overlapping sequences are accepted. Design a logic circuit using JK flip-flops.

(15 marks)

5. (a) Define and explain the following digital IC terminologies :

(i) Fan out. (ii) Propagation delay.

(iii) Noise immunity. (iv) Current sourcing and current sinking logic.

(v) Speed-power product.

Give typical values of the above both TTL and CMOS ICs.

Or

(b) Draw a neat sketch of bipolar memory cell and explain its operation. Also explain how an $m \times n$ capacity memory is built using above cells. Differentiate between static and dynamic memories.

(15 marks)

[4 × 15 = 60 marks]