D 1825

(2 Pages)

Name.....

Reg. No.....

THIRD SEMESTER B.Tech. (ENGINEERING) DEGREE EXAMINATION DECEMBER 2004

(New Scheme)

CS/IT 2K 305/PTCS 2K 304—SWITCHING THEORY AND LOGIC DESIGN

Time : Three Hours Maximum : 100 Marks

I. (a) Convert $(268.75)_{10}$ to binary, octal and hexadecimal.

(b) Reduce the following function using Karnaugh map, $F(a, b, c, d) = \Sigma m(0, 1, 4, 8, 9, 10)$.

(c) Implement the following Boolean function with NAND-NAND logic :

$Y = AC + ABC + A'BC + AB + D$

(d) Implement $F(A, B, C) = \Sigma(1, 3, 5, 6)$ with a 4 × 1 multiplexer.

(e) Give the singular cover for a 2 input EXOR gate and 2 input AND gate.

(f) What is Programmable Logic Array ? How it differs from ROM ?

(g) Draw the logic diagram of SR flip flop using NOR gate and give its truth table.

(h) Mention few applications of Shift registers.

(8 × 5 = 40 marks)

II. (a) (i) Simplify the following Boolean expression :—

$F = [(a' + d' + b'c)(b + d + ac')]' + b'c'd' + a'c'd.$

(ii) Simplify the following Boolean expression :—

$F = (AB + C + D)(C' + D)(C' + D + E).$

(iii) Prove that $(a + b)(a' + c)(b + c) = (a + b)(a' + c)$ using the basic theorems of Boolean algebra.

(4 + 4 + 7 = 15 marks)

Or

(b) (i) Find the minterm and maxterm expansion of the following :—

$f(a, b, c, d) = a'(b' + d) + acd'$

(ii) Simplify $F(A, B, C, D) = \Sigma m(0, 1, 2, 4, 8, 9, 10)$ in :

(1) Sum of Products form.

(2) Product of Sums form.

(7 + 8 = 15 marks)

Turn over

III. (a) Design a BCD to gray code converter. (15 marks)

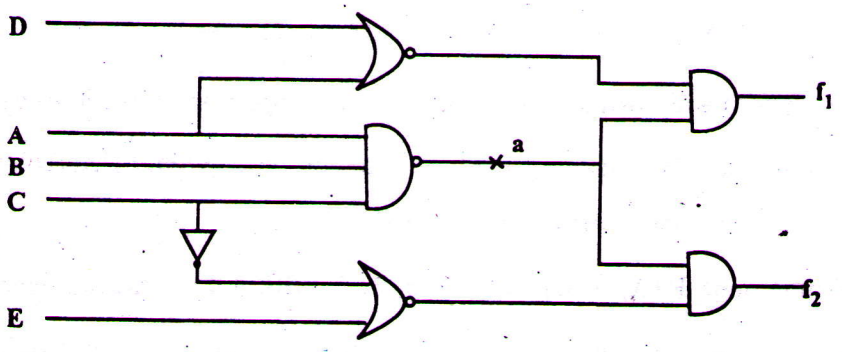
Or

(b) (i) Design parity generator to generate even and odd parity (for 3 bit message).

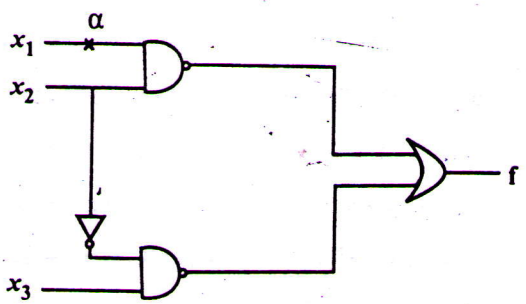
(ii) Design and implement the circuit for parity checker (for 4 bit message).

(10 + 5 = 15 marks)

IV. (a) (i) Using path sensitisation method, derive the test set for the given circuit, for $\alpha = a/1$.



(ii) Using Boolean difference method, find the test set of $\alpha = x_1/1$.



(8 + 7 = 15 marks)

Or

(b) Implement the following Boolean functions using PLA :—

$F_1 (A, B, C) = \Sigma m (0, 1, 3, 5)$

$F_2 (A, B, C) = \Sigma m (0, 3, 5, 7)$

(15 marks)

V. (a) Design a MOD-5 synchronous counter using JK flip flops and implement it. (15 marks)

Or

(b) With neat diagram, explain 4 bit serial in serial out shift register. (15 marks)

[4 × 15 = 60 marks]