D 1819

(2 pages)

Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION

DECEMBER 2004

EC-2K-305/AI-2K-305 – DIGITAL ELECTRONICS

(New Scheme)

Time : Three Hours

Maximum : 100 Marks

I. (a) X = 1010100 Y = 1000011, perform the subtraction (a) X–Y, (b) Y–X using (i) 1's complement and (ii) 2's complement.

(b) Express the Boolean function $F = xy + \bar{x}z$ in product of max term.

(c) Construct a half adder and a half subtractor.

(d) Generate EX-NOR function using only NOR gates.

(e) Construct Master-Slave JK flip-flop.

(f) Draw the block diagram of a three-decade decimal BCD counter.

(g) Define the terms : Fan out, Power dissipation and Propagation delay.

(h) Draw CMOS-NAND gate.

(8 × 5 = 40 marks)

II. (a) Simplify the following Boolean function by means of tabulation method :–

P(A, B, C, D, E, F, G) = Σ (20, 28, 38, 39, 52, 60, 102, 103, 127) (15 marks)

Or

(b) (i) Draw the logic diagram of 3 to 8 line decoder. (7 marks)

(ii) Construct a 4 × 16 decoder with two 3 × 8 decoders. (8 marks)

III. (a) Construct 4-bit ripple up-down counter. (15 marks)

Or

(b) Draw the logic diagrams of J-K and RS flip-flops. (15 marks)

IV. (a) Design a sequential circuit with two D flip-flops, A and B and one input x. When $x = 0$, the state of the circuit remains the same. When $x = 1$, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00 and repeats. (15 marks)

Or

(b) Discuss the state table reduction procedure with an example. (15 marks)

Turn over

V. (a) Discuss the operation of open collector TTL gate. (15 marks)

Or

(b) Discuss the operation of ECL with neat circuit diagram. (15 marks)

(4 × 15 = 60 marks)