JYOTHI ENGG. COLLEGE LIBRARY
THRISSUR EDUCATIONAL TRUST
CHERUTHURUTHY

D 1681

Name.....

Reg. No.....

SEVENTH SEMESTER B.TECH. ENGINEERING DEGREE EXAMINATION
NOVEMBER 2004

Computer Science

CS 2K 702—COMPUTER ARCHITECTURE

(New Scheme)

Time : Three Hours Maximum : 100 Marks

Answer **all** *the questions.*

I. (a) Explain the major hurdles of pipelining.

(b) Describe the instruction format of DLX.

(c) Explain Instruction-level parallelism.

(d) List the primary components of the instruction set architecture of DLXV.

(e) Differentiate between cache and virtual memory.

(f) Explain throughput versus response time for a typical I/O system.

(g) Explain shared versus switched media of connecting computers.

(h) Draw the basic structure of a centralized shared memory multiprocessor and explain.

(8 × 5 = 40 marks)

II. (a) Explain how measuring and reporting the performance of a system is done.

Or

(b) Explain with examples the different addressing modes of a computer system.

III. (a) Describe the hardware support required for extracting more parallism for ILP.

Or

(b) Describe the different measures of performance for vector processors.

IV. (a) Explain how protection of virtual memory is done in the Intel pentium systems.

Or

(b) What is meant by reliability and availability ? Describe the different RAID levels.

V. (a) Explain the two practical issues to be considered for interconnection networks.

Or

(b) Explain the two models for memory consistency of a multiprocessor.

(4 × 15 = 60 marks)