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Name.....

Reg. No.....

SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION DECEMBER 2005

CS 2K 702—COMPUTER ARCHITECTURE

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Section I

I. (a) Discuss the different classes of instruction sets with suitable examples.

(b) What is pipelining ? What are hazards ? Brief the pipeline hazards.

(c) Explain instruction level parallelism.

(d) Explain the concept of chaining in vector processors.

(e) Explain how a block is identified if it is in the cache ?

(f) Describe the techniques used for Fast Address Translation in brief.

(g) Differentiate between circuit switched and packet switched networks.

(h) Draw the basic structure of a centralized shared memory multiprocessor and explain.

(8 × 5 = 40 marks)

Section II

II. (a) Explain how measuring and reporting the performance of a system is done. (15 marks)

Or

(b) (i) Explain the major types of optimizations performed by modern compilers with examples. (12 marks)

(ii) Define : latency and initiation interval. (3 marks)

III. (a) Discuss the different types of dependences on achieving instruction level parallelism. (15 marks)

Or

(b) Describe the different measures of performance for vector processors. (15 marks)

IV. (a) Discuss the various organizations for improving main memory performance. (15 marks)

Or

(b) Describe the different RAID levels. (15 marks)

V. (a) (i) Explain the basic schemes for Enforcing Coherence. (7 marks)

(ii) Explain Synchronization and the basic hardware primitives required to implement synchronization. (8 marks)

Or

(b) Discuss the two practical issues to be considered for interconnection networks. (15 marks)

[4 × 15 = 60 marks]