

C 6266



Name.....

Reg. No.....

**SIXTH SEMESTER B.TECH. (ENGINEERING)
DEGREE EXAMINATION, JUNE 2005**

EC 2K 606 B—HIGH SPEED DIGITAL DESIGN

Time : Three Hours

Maximum : 100 Marks

- I. (a) Explain the capacitance effect in high speed digital circuits.
(b) Define and explain :
 1 Rise time.
 2 Bandwidth of oscilloscope probes.
(c) Explain the following :
 1 Propagation delay.
 2 Layer stacking.
(d) What is Vias ? Explain.
(e) Explain the mechanical properties of vias.
(f) What is slotted ground plane ? Explain.
(g) What is clock skew ? Explain.
(h) How the cross-talk on clocklines is controlled ? Explain.

(8 × 5 = 40 marks)

- II. (a) Describe in detail the role of time and distance in high speed digital circuits.

Or

- (b) Explain in detail the high speed properties of logic gates.

- III. (a) Explain the following :

- 1 Infinite uniform transmission lines.
- 2 Special transmission line cares.

Or

- (b) Explain the effect of cross-talk in solid ground planes and crosshatched ground planes.

- IV. (a) Explain in detail the various types of transmissions.

Or

- (b) Describe in detail the properties of vias.

- V. (a) Write short notes on :

- 1 Stable reference voltage.
- 2 Clock distribution.

Or

- (b) Describe in detail the methods to reduce clock skew.

(4 × 15 = 60 marks)