

D 27255

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Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE
EXAMINATION, DECEMBER 2006

EC/AI 2K 305—DIGITAL ELECTRONICS

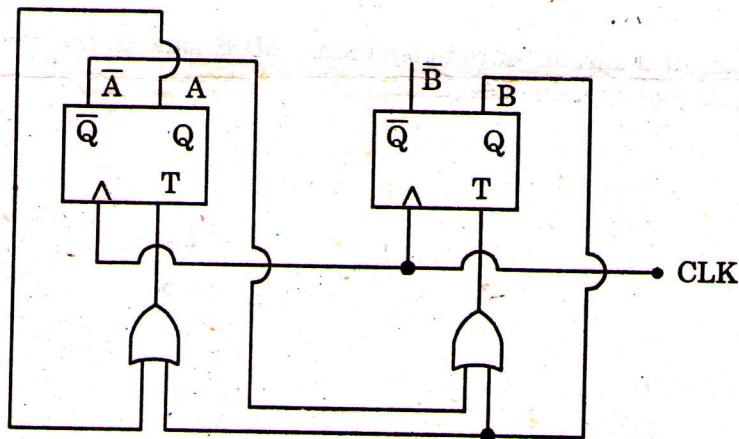
Time : Three Hours

Maximum : 100 Marks

Answer all questions.

Part A

- (a) Simplify the following expressions using Boolean identities :—
 - (i) $Y = \overline{A} \overline{B} C D + A B C D + \overline{A} \overline{C} \overline{D} + \overline{A} C \overline{D} + A \overline{B} \overline{D}$.
 - (ii) $Y = A B C D + \overline{A} \overline{B} \overline{C} \overline{D} + A \overline{B} \overline{C} + B C$.
- (b) Draw 8 : 1 multiplexer using NAND only and explain.
- (c) Draw full adder circuit and explain.
- (d) Draw the circuit diagram of Johnson counter and explain.
- (e) Derive the state table of the following sequential circuit :—



- (f) Explain what is meant by state diagram.
- (g) Explain what is meant by (i) Noise immunity ; (ii) Logic flexibility.
- (h) What is meant by static memory and dynamic memory ? Explain.

(8 × 5 = 40 marks)

Part B

2. (a) Reduce the following logic function using tabular method and realize it using basic gates :—

$$Y = \sum m (0, 2, 6, 7, 8, 10, 12, 14, 15, 52).$$

Or

- J (b) Design a combinational logic circuit to convert BCD to excess-3 code.

Turn over

3. (a) (i) Design a full subtractor using NAND only.

(8 marks)

- (ii) Draw the circuit diagram of BCD counter and explain.

(7 marks)

Or

- (b) Draw the block diagram of divider unit and explain its operation.

4. (a) Design a sequential circuit described by the following state equations. Use JK flip-flops.

$$A(t+1) = \bar{A} \bar{B} C D + \bar{A} \bar{B} C + A C D + A \bar{C} \bar{D}$$

$$B(t+1) = \bar{A} C + C \bar{D} + \bar{A} B \bar{C}$$

$$C(t+1) = B$$

$$D(t+1) = \bar{D}$$

Or

- (b) Design a sequential logic circuit to generate the following repeated random sequences :

1, 3, 7, 2, 5, 1, 3

(8 marks)

5. (a) (i) Draw the transfer characteristic of ECL logic gate and explain.

(7 marks)

- (ii) Explain what is meant by fan-in and fan-out of logic diagram.

Or

- (b) Draw the circuit diagrams of complementary MOS logic (i) inverter ; (ii) NAND gate ; and

- (iii) NOR gate and explain operations.

(5 + 5 + 5 = 15 marks)

[4 × 15 = 60 marks]