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D 27180 (Pages : 2) Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2006

EC/AI/IC 2K 506 D—DIGITAL SYSTEM DESIGN

Time : Three Hours Maximum : 100 Marks

Answer **all** *the questions.*

1. (a) Check whether the circuit realized by the function $Y = (x_1 x_2 + x_2' x_3)$ possesses hazard. If so suggest suitable scheme to make it hazard free.

   (b) What is meant by clock skew ? What will be its effect on the function of the circuit ?

   (c) Discuss about compilation and simulation of VHDL code.

   (d) What is meant by operator over loading ? What for it is used ?

   (e) Draw the schematic of PAL and PLA in block diagram form and explain the difference between them.

   (f) With the help of schematic explain the structure of 3 input LUT used in the CLB of an FPUA at chip and explain how it can be used to implement a logic function of 3 variables.

   (g) Discuss about *s-a*-0 and *s-a*-1 fault models.

   (h) How multilevel networks are tested for internal node fault ?

   (8 × 5 = 40 marks)

2. (a) Design a synchronous sequential circuit to meet the following specifications :—

   The circuit has one input, w and one output, z. All changes in the circuit occurs on the positive edge of a clock signal. The output $z = 1$ if during two immediately preceding clock cycles the input w was equal to 1. Otherwise to value of $z = 0$.

   (15 marks)

   Or

   (b) Explain the following :—

   (i) Conversion of asynchronous data input to synchronous input data. (6 marks)

   (ii) Metastable state. (4 marks)

   (iii) Set up and hold time of flip-flop. (5 marks)

3. (a) Discuss about the VHDL operators and VHDL functions.

   Or

   (b) Write the VHDL model for 8 bit counter.

4. (a) Draw the simplified architecture of altera 7000 series internal architecture. Also explain the macrocell details.

   Or

Turn over

(b) Draw the PLD implementation of the function

$$f(x_1, x_2, x_3, x_4, x_5, x_6, x_7) = x_1 \bar{x}_3 x_6 + x_2 x_4 x_5 + \bar{x}_1 x_2 x_3 x_7 + \bar{x}_5 x_6 x_7 + x_1 \bar{x}_3 x_5 x_7.$$

Also explain why SOP form is best suited for PLD/CPLD implementation and multilevel implementation is best suited for FPUA implementation.

5. (a) Explain boundary scan test methodology.

Or

(b) Discuss about :

(i) Self test circuit for RAM.

(ii) Built in Logic Block Observation (BILBO).

(4 × 15 = 60 marks)