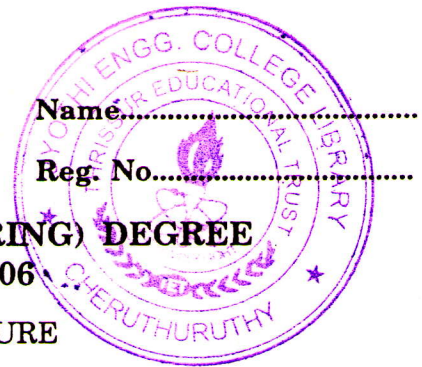


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**SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE
EXAMINATION, DECEMBER 2006**

CS 2K 702—COMPUTER ARCHITECTURE

Time : Three Hours

Maximum : 100 Marks

Answer all questions.

Section I

1. (a) Suppose we are considering two alternatives for our conditional branch instructions, as follows :

CPU A : A condition code is set by a compare instruction and followed by a branch that tests the condition code.

CPU B : A compare is included in the branch.

On both CPUs, the conditional branch instruction takes 2 cycles, and all other instructions take 1 clock cycle. On CPU A, 20 % of all instructions executed are conditional branches : since every branch needs a compare, another 20 % of the instructions are compares. Because CPU A does not have the compare included in the branch, assume that its clock cycle time is 1.25 times faster than that of CPU B. Which CPU is faster ? Suppose CPU A was only 1 : 1 times faster ?

- (b) Highlight the advantages and disadvantages of GPR architecture.
- (c) Explain how data hazards are overcome by dynamic scheduling.
- (d) Explain the basic structure of a vector-register architecture.
- (e) Differentiate between Cache and Virtual memory.
- (f) Explain in brief the operation of a Cache memory.
- (g) Define : Time of flight, Transport latency, Sender overhead and Receiver overhead.
- (h) Explain Multiprocessor Cache Coherence.

(8 × 5 = 40 marks)

Section II

2. (a) Discuss in brief the major hurdles of pipelining. (15 marks)

Or

- (b) (i) Describe the instruction format of DLX. (5 marks)
- (ii) Discuss in brief instruction encoding and its basic variations. (10 marks)

3. (a) Describe the hardware support required for extracting more parallelism for ILP.

Or

- (b) Explain the techniques for improving the performance of vector processors. (15 marks)

Turn over

Handwritten calculations:
$$\begin{array}{r} 282 \\ 55 \\ \hline 337 \end{array}$$

Handwritten calculations:
$$\begin{array}{r} 282 \\ 125 \\ \hline 407 \end{array}$$

4. (a) Explain how protection of virtual memory is done in the Intel Pentium systems.

Or

(b) Discuss any *three* techniques for reducing Cache misses.

(15 marks)

5. (a) (i) Explain the simple network connecting two machines.

(10 marks)

(ii) Describe the switch topologies in brief.

(5 marks)

Or

(b) Explain the two models for memory consistency of a multiprocessor.

(15 marks)

[4 × 15 = 60 marks]