C 20560

Name.....

Reg. No.....

SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2006

EC 2K 606 (B)—HIGH SPEED DIGITAL DESIGN

Time : Three Hours

Maximum : 100 Marks

Answer **all** *questions.*

I. (a) Explain the loading effects of Oscilloscope probes.

(b) State and explain the advantages of high speed digital design.

(c) What is meant by infinite uniform transmission line ? Explain its characteristics.

(d) What is layer stacking ? Explain.

(e) Explain the cross-talk in terminators.

(f) What is meant by inductance of Vias ? Explain.

(g) What are the methods to reduce clock skew ? Explain any *one* method.

(h) Explain the steps to choose a by-pass capacitor.

(8 × 5 = 40 marks)

II. (a) Describe in detail the high speed properties of logic gates.

Or

(b) Explain in detail the principle of signal pickup in Oscilloscope probes.

III. (a) Explain the properties and characteristics of Uniform transmission lines.

Or

(b) Explain the following :—

1 Near and far end cross-talk.

2 Point to point wiring.

IV. (a) Explain in detail the properties of Vias.

Or

(b) Describe in detail the capacitance of Vias.

V. (a) What is Clock skew ? Explain it in detail.

Or

(b) Write technical notes on :

1 Clock jitter.

2 Controlling cross-talk on clock lines.

(4 × 15 = 60 marks)