

## SIXTH SEMESTER B.TECH. (ENGINEERING) DECREE EXAMINATION, JUNE 2006

## EC/AI/IC 2K 604—DIGITAL SIGNAL PROCESSING

Time: Three Hours

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## Answer all questions.

- I. (a) State and prove any one property of DFS.
  - (b) (i) What is twiddle factor? Explain.

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(ii) Draw the basic butterfly diagram for decimation-in-time radix-2 FFT algorithm and explain.

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(3 marks)

(c) Draw the FIR linear phase and cascade realization of the system function

$$H(z) = \left(1 + \frac{1}{2}z^{-1} + z^{-2}\right)\left(1 + \frac{1}{4}z^{-1} + z^{-2}\right).$$

- (d) Explain about zero-input limit cycle oscillations.
- (e) Describe bilinear transformation mapping technique.
- (f) Explain the design procedure of FIR filter using window function.
- (g) Compare TMS 320 family with ADSP 2100 family.
- (h) Explain about general purpose digital signal processor.

 $(8 \times 5 = 40 \text{ marks})$ 

II. (a) State and prove convolution property of DFT.

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- (b) Using decimation-in-time radix-2 FFT algorithm evaluate the 8-point DFT of  $x(n) = \{1, -1, 1, -1, 2, -2, 2, -2\}$ .
- III. (a) Draw the cascade and parallel realizations for the following system function:

H (z) = 
$$\frac{1 + \frac{1}{4}z^{-1}}{\left(1 + \frac{1}{2}z^{-1}\right)\left(1 + \frac{1}{2}z^{-1} + \frac{1}{4}z^{-2}\right)}.$$

Or

(b) Explain quantization in floating point realization of IIR digital filters.

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IV. (a) Design a digital Butterworth filter to meet the following constraints:

$$\frac{1}{\sqrt{2}} \le |H(w)| \le 1$$
, for  $0 \le w \le 0.2\pi$ 

 $0 \le |H(w)| \le 0.1$ , for  $0.5 \pi \le w \le \pi$ using impulse invariant mapping.

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- (b) Design a bandpass filter which approximates the ideal filter with cut off frequency at 0.2 rad/sec and 0.3 rad/sec. The filter order is N = 7. Use Hanning window function.
- V. (a) Explain about:

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- (i) Pipelining.
- (ii) Hardware multiplier.

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(b) Explain the architecture of TMS 320 C 50 DSP processor with neat block diagram.

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 $[4 \times 15 = 60 \text{ marks}]$