D 42034 (Pages : 2) Name.....

Reg. No.....

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2007

AI/BM 04 305—DIGITAL SYSTEMS

(2004 Admissions)

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Part A

1. State and explain De Morgan's theorems.
2. Prove the universal property of NOR and NAND gates.
3. Implement $f = \sum m$ (2, 3, 7, 9) using 4 × 1 MUX.
4. Explain SOP and POS forms. Get the corresponding POS equation of $f = \sum m$ (2, 3, 7, 9).
5. Explain the concept of universal shift register.
6. Explain the principle and application of tri-state logic gates.
7. Draw the state table, state diagram and characteristics equation of JK flip-flop.
8. Differentiate between synchronous and asynchronous sequential circuits.

(8 × 5 = 40 marks)

Part B

9. (a) Find the reduced SOP and POS that are equivalent to E $(w, x, y, z) = \prod$ M (1, 3, 4, 7, 10, 13, 14, 15).

Or

(b) Explain the principle of error detection and error correction with numerical examples. Explain one technique each for detection and correction.

10. (a) Draw the circuit of 2 digit BCD adder and explain. Explain the methods for speed improvement in adders.

Or

(b) Draw the circuit of JK flip-flop using NAND gates alone. What is race around condition in it ? Clearly explain two methods to eliminate the problem.

Turn over

11. (a) Design a decimal up/down asynchronous counter using JK flip-flop. Draw the $\bar{Q}$ outputs and explain.

Or

(b) Draw the circuit of a TTL totem pole NAND gate. Explain the role of every component in the circuit. Compare TTL and ECL logic families. What are the principle advantages of TTL ?

12. (a) Differentiate between Moore and Mealy machines with examples for each.

Or

(b) Design a synchronous counter to pass through ... 1, 3, 5, 6, 8, 10, 12..... using SR flip-flop. The counter should be free from lockout. Give its state table and state diagram.

(4 × 15 = 60 marks)