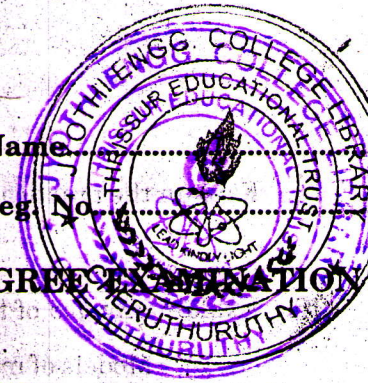


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Name

Reg. No.



**SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION
DECEMBER 2007**

CS 2K 702—COMPUTER ARCHITECTURE

(New Scheme)

Time : Three Hours

Maximum : 100 Mark

Section A

1. Explain the major data and control hazards of DLX.
2. Write in short the task of a computer designer.
3. Discuss on the dynamic hardware prediction.
4. Explain Instruction level parallelism.
5. Differentiate between main and virtual memory.
6. Explain how virtual memory protection is achieved in Intel Pentium.
7. Brief the features of Interconnection networks.
8. Draw the basic structure of a centralized shared memory processor and explain.

(8 × 5 = 40 marks)

Section B

9. Explain the DLX architecture in detail. (15 marks)
Or
10. Explain the instruction set architecture and its classification in detail. (15 marks)
11. Discuss the hardware support required for extracting more parallelism for ILP. (15 marks)
Or
12. Explain in detail the vector architecture and its performance measures. (15 marks)
13. Discuss in detail the design of a I/O system and its performance measures. (15 marks)
Or
14. (a) Explain the cache memory organization. (7 marks)
(b) Discuss in brief the UNIX file system. (8 marks)

Turn over

plain the practical issues to be considered for interconnection networks.

(15 marks)

Or

plain any two of the following :—

- (a) Models of memory consistency.
- (b) Synchronization.
- (c) Application domains.

(2 × 7½ = 15 marks)

[4 × 15 = 60 marks]