C 32076 (Pages : 2) Name.....

Reg. No.....

SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2007

IT 2K 605—COMPUTER ARCHITECTURE

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

1. (a) Classify the optimizations performed by modern compilers.
   (b) What are the issues involved in displacement and immediate addressing modes ?
   (c) Discuss handling of Vector Stride in Vector Computing.
   (d) What are the factors that limit instruction level parallelism ?
   (e) What are the factors favouring large page size ?
   (f) Define the terms :
      (i) Cache hit.
      (ii) Hit ratio.
   (g) What are the advantages of shared memory and message passing communication ?
   (h) Discuss Cache coherence problem.

(8 × 5 = 40 marks)

2. (a) (i) Discuss different pipeline hazards. (7 marks)
   (ii) Explain the concept of pipelining the multicycle operations. (8 marks)

Or

   (b) (i) Discuss encoding an instruction set with an example. (7 marks)
   (ii) State and explain the importance of Andahl's law. (8 marks)

3. (a) (i) What are the limitations of ILP that are applicable even to a perfect model ? (7 marks)
   (ii) What is meant by two level predictors ? Explain with an eg. (8 marks)

Or

   (b) (i) Write notes on vector architecture. (7 marks)
   (ii) Discuss any *two* dynamic scheduling algorithms. (8 marks)

4. (a) (i) Explain any *two* techniques for reducing Cache miss rate. (7 marks)
   (ii) Discuss various Virtual Memory Management Schemes. (8 marks)

Or

   (b) (i) What are the main goals of RAID technology ? Discuss different RAID organisations. (8 marks)
   (ii) What is meant by split transaction ? Explain. (7 marks)

Turn over

5. (a) (i) Discuss how routing is done in switched media. (8 marks)

(ii) Explain the concept of snooping protocol for Cache coherence. (7 marks)

Or

(b) (i) Discuss the architecture of distributed shared memory and its implementation. (8 marks)

(ii) What is false sharing ? Explain. (7 marks)

[4 × 15 = 60 marks]