C 31982 (Pages 2)

Name.....

Reg. No.....

SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2007

EC/AI/IC/BM 04 602—DIGITAL SIGNAL PROCESSING

(2004 Admissions)

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Part A

I. (a) Find the 4-point DFT of $x(n) = \{1, 0, 1, 0\}$.

(b) Explain how do you determine DFT of 2 real sequence efficiently.

(c) What are the advantages of lattice structure ? Explain.

(d) Explain the effects of coefficient of quantization FIR filter.

(e) Explain the design procedure of FIR filter using window functions.

(f) Derive the mapping formula for designing IIR filter using approximate derivatives.

(g) Explain MAC configuration in DSPs.

(h) Explain what is meant by very-long instruction word.

Part B

II. (a) Using FFT algorithm, evaluate DFT coefficients of the discrete sequence :

$x(n) = \{1, 2, 3, 4, 5, 6, 7, 8\}$.

Or

(b) Explain split-radix FFT algorithm for evaluating DFT coefficients.

III. (a) Derive frequency response of linear phase FIR filter of length 15 with (i) anti symmtric condition and (ii) symmetric condition.

Or

(b) (i) Explain what is meant by truncation errors and round off errors. (5 marks)

(ii) Study the limit cycle behaviour of the system having difference equation :

$$y(n) = 0.95\, y(n-1) + x(n)$$

for $x(n) = 0$.

Turn over

IV. (a) Design a linear phase digital FIR filter for the following specifications :—

Pass band : (2000 – 4000) Hz

Sampling frequency F_s = 10000 Hz.

Window Function : Hamming

Order of the filter N = 11.

Or

(b) Convert the following analog transfer function into digital using,

(i) bilinear transformation.

(ii) impulse invariant mapping $H(s) = \frac{2}{(s + 0.9)^2 + 4}$.

Assume sampling rate = 1 Hz.

V. (a) Draw the block diagram of architecture of fixed point DSP processor and explain.

Or

(b) (i) Explain the concept of pipelining with clock diagram. (7 marks)

(ii) Draw the block diagram of hardware multiplier accumulator and explain. (8 marks)

[4 × 15 = 60 marks]