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Name: _____

Reg. No. _____



**FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION
JUNE 2007**

EC 04 403—DIGITAL ELECTRONICS

(2004 admissions)

Time : Three Hours

Maximum : 100 Marks

Answer all questions.

- I. (a) Name the universal logic gates. Construct an Ex-OR gate using only NAND gates.
(b) Write short notes on ASC11 code.
(c) Draw the TTL gate with totem-pole output.
(d) Write the concept of ring counter.
(e) What is meant by race condition ?
(f) Draw the basic blocks of ASM chart.
(g) Write the significance of Hazard.
(h) What is meant by "edge triggering" ? Explain.
(8 × 5 = 40 marks)
- II. (a) Simplify the Boolean function F together with the don't care conditions d in sum of products and product of sums :
$$F(A, B, C, D) = \sum (3, 4, 13, 15)$$
$$d(A, B, C, D) = \sum (1, 2, 5, 6, 8, 10, 12, 14)$$

(15 marks)
Or
- (b) Explain fixed point and floating point representation with examples. (15 marks)
- III. (a) Draw the circuit of ECL and explain. (15 marks)
Or
- (b) Explain the basic principle of $4 \times 1 = 4$ multiplexer with a neat logic diagram. (15 marks)
- IV. (a) Design a digital system with three 4-bit registers, A, B and C to perform the following operations :—
(i) Transfer two binary numbers to A and B when a start signal is enabled.
(ii) If $A > B$, shift left the contents of A and transfer the result to register C.
(iii) If $A < B$, shift right the contents of B and transfer the result to register C.
(iv) If $A = B$, transfer the number to register C unchanged.
(15 marks)
Or
- (b) Explain Mealy and Moore state models with examples. (15 marks)
- V. (a) Discuss the state reduction in asynchronous sequential circuits. (15 marks)
Or
- (b) Discuss the state assignment using additional state variables. (15 marks)
(4 × 15 = 60 marks)