D 51557 (Pages 2) Name.....

Reg. No.....

FIFTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2008

EE 2K 504/PTEEE 2K 404—PULSE AND DIGITAL ELECTRONICS

Time : Three Hours Maximum : 100 Marks

Part A

1. Answer *all* questions :

   (a) Draw the waveforms of a collector coupled monostable multivibrator.

   (b) What are methods of generating a time base waveform ?

   (c) State and prove DeMorgan's laws.

   (d) Implement the function $F = \overline{AB + CD + E}$ using :

      1 CMOS logic

      2 NMOS logic with depletion NMOS load.

   (e) Design a 3 bit binary to gray code converter.

   (f) Realize the function given below using a 4 × 1 multiplexer $F = \Sigma m(1, 2, 5, 6, 7)$.

   (g) Mention the applications of shift registers.

   (h) Draw the state diagram for a mealy type serial adder.

(8 × 5 = 40 marks)

Part B

2. (a) (i) Explain in detail about diode reverse recovery time. (10 marks)

   (ii) Discuss various switching times of a BJT when driver by a pulse waveform. (5 marks)

Or

   (b) Explain the working of a collector coupled astable multivibrator with a neat circuit diagram.

3. (a) Explain working of a TTL gate with TOTEM output. Compare its features with open collector TTL gate.

Or

   (b) (i) Draw the circuit for ECL 2 input OR/NOR gate and explain its working. (10 marks)

   (ii) State and prove DeMorgan's theorem. (5 marks)

4. (a) (i) Create a circuit to generate parity bits for a four bit message using Hamming code. Assume odd parity format.

(8 marks)

   (ii) Realize the function $F = \Sigma m(1, 4, 6, 7)$ using 74LS138 decoder and NAND gates only.

(7 marks)

Or

Turn over

(b) (i) Design a 4 bit magnitude comparator using a 4 bit parallel binary adder and suitable gates.

(10 marks)

(ii) Find Minimal SOP expression for $F = \Sigma m(1, 3, 6, 7, 8, 10, 12)$ using K-map.

(5 marks)

5. (a) (i) Design a circuit to convert square pulses of frequency 1 kHz into square pulses of frequency 125 Hz.

(10 marks)

(ii) Write short notes on Static RAM and Dynamic RAM. (5 marks)

Or

(b) Design a sequence detector to detect the sequence "011" or "100". Assume overlapping sequences. Implement the circuit using T flip flops.

(15 marks)

[4 × 15 = 60 marks]