

D 51490

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2008

CS/IT 04 305 - SWITCHING THEORY AND LOGIC DESIGN

(2004 Admissions)

Time	:	Three	Hours
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Maximum: 100 Marks

- I. (a) Discuss the postulates of Boolean Algebra.
 - (b) Simplify the function $Y = B(\overline{A} + \overline{C}) + \overline{A}\overline{B}$ and draw the logic circuit for the simplified function.
 - (c) Explain why NOR gate is known as an universal gate.
 - (d) Derive logic expressions for sum and carry of a full adder.
 - (e) Write a brief note on Fault Classes.
 - (f) What do you mean by Design for Testability?
 - (g) How will you modify a SR flip-flop to a JK flip-flop?
 - (h) Explain the basic concept of a Shift Register.

 $(8 \times 5 = 40 \text{ marks})$

II. (a) Reduce the following Boolean Function using Quine McCluskey method.

 $F(A, B, C, D, E) = \Sigma(0, 1, 4, 5, 6, 7, 12, 18, 19, 22, 23, 28, 31)$

(15 marks)

(b) Write short notes on the following: (i) Electronic Gates and mechanical contacts; (ii) Normal and canonical forms.

(10 + 5 = 15 marks)

Or

III. (a) With the help of neat diagram explain the principle of look ahead adder. What are its advantages?

(b) Explain the differences between multiplexers and Demultiplexers with the help of neat logic diagrams.

(15 marks)

IV. (a) Explain the path sensitisation method with an example.

(15 marks)

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(b) Write short notes on the following: (i) Fault Diagnosis and Testing; (ii) Essential prime cube theorem.

(8 + 7 = 15 marks)

V. (a) Design a 4-bit ripple up counter and explain.

(15 marks)

Or

(b) Write short notes on the following: (i) Triggering of Flip-Flops; (ii) Synchronous counters.

(8 + 7 = 15 marks)

 $[4 \times 15 = 60 \text{ marks}]$