D 51438

THIRD SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2008

CS 2K 305/IT 2K 305/PTCS 2K 304—SWITCHING THEORY AND LOGIC DESIGN

Time : Three Hours   Maximum : 100 Marks

I.   (a)   State and prove DeMorgan's theorem with three variables.

     (b)   Simplify the Boolean function with Karnaugh map :

         $F (A, B, C, D) = \Sigma (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$

     (c)   Construct Half adder using only NAND gates.

     (d)   Write short notes on parity generators.

     (e)   Explain Fault classes.

     (f)   Write short notes on Path sensitisation method.

     (g)   Write short notes on triggering the flip-flops.

     (h)   Explain the operation of JK flip-flop with internal gates.

                                        $(8 \times 5 = 40$ marks$)$

II.   (a)   The sum of all the min-terms of a Boolean function of n variables is equal to 1. Prove the above statement for $n = 3$. Suggest a procedure for a general proof.

                                        (15 marks)

Or

     (b)   Simplify the following Boolean function by tabulation method :

         $P (A, B, C, D, E, F, G) = \Sigma (20, 28, 38, 39, 52, 60, 102, 103, 127)$

                                        (15 marks)

III.   (a)   Design a combinational circuit with three inputs and six outputs. The output binary number should be the square of the input binary number.

                                        (15 marks)

Or

     (b)   (i)   Explain the principle of Multiplexer with an example.   (8 marks)

         (ii)   Explain the concept of demultiplexer with an example.   (7 marks)

IV.   (a)   Explain PLA minimization with an example.   (15 marks)

Or

     (b)   Explain Fault diagnosis and testing.   (15 marks)

V.   (a)   Construct a 4-bit binary ripple up-down counter with JK flip-flops.   (15 marks)

Or

     (b)   Discuss the principle of shift registers and their applications.   (15 marks)

                                        $[4 \times 15 = 60$ marks$]$