D 51309 (Pages 2)

Name .....

Reg. No .....

SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, DECEMBER 2008

CS 2K 702—COMPUTER ARCHITECTURE

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Section A

1. Describe the instruction format of DLX.
2. Write short notes on the task of a computer designer.
3. Explain how vector performance can be enhanced.
4. Discuss the advantages of instruction level parallelism.
5. Discuss on the issues of reducing hit time.
6. Explain the terms reliability and availability related to I/O systems.
7. Discuss on Interconnection networks.
8. Explain shared versus switched media of connecting computers.

(8 × 5 = 40 marks)

Section B

9. Explain how measuring and reporting the performance of a system is done. (15 marks)

Or

10. (a) Explain the process of encoding an instruction. (5 marks)

    (b) List and explain the primary components of the instruction set architecture of DLXV. (10 marks)

11. Discuss in detail the vector architecture. (15 marks)

Or

12. Explain dynamic scheduling and dynamic hardware prediction. (15 marks)

13. (a) Explain throughput versus response time for a typical I/O system. (7 marks)

    (b) Differentiate between virtual memory and cache memory. (8 marks)

Or

Turn over

14. (a) Describe in brief the UNIX file system. (10 marks)

(b) Write short notes on I/O system. (5 marks)

15. Explain the practical issues to be considered for interconnection networks. (15 marks)

Or

16. (a) Explain the distributed shared memory architecture in detail. (10 marks)

(b) Discuss on memory consistency. (5 marks)

[4 × 15 = 60 marks]