C 48868 (Pages : 2) Name.....

Reg. No.....

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION JUNE 2008

EC 04 403—DIGITAL ELECTRONICS

(2004 admissions)

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Part A

I. (a) Convert the following logic function into max. terms :

$$Y = (A + B)(B + C)(C + D)(D + E)$$

(b) Explain unsigned adder and subtractor circuit.

(c) List the characteristics of digital ICS.

(d) Draw the circuit of edge triggered D flip-flop and explain.

(e) Explain about Mealy stage model.

(f) Describe the design procedure for asynchronous sequential circuit.

(g) What is dynamic hazards ? Explain.

(h) How do you eliminate static hazard in an asynchronous circuit ? Explain.

(8 × 5 = 40 marks)

Part B

II. (a) Using Karnaugh map simplify the following logic function and realise using logic gates.

$$Y = \sum m(5, 6, 7, 8, 9) + \sum d(10, 11, 12, 13, 14, 15)$$

Or

(b) Draw the block diagram of 4-bit carry-look ahead adder and explain its operation.

III. (a) Draw the NAND and NOR logic circuit using CMOS and explain its operation.

Or

(b) Draw the circuit of 4-bit binary counter using J.K. flip-flop and explain its operation with timing diagram.

Turn over

IV. (a) For the following table, assume that the unspecified outputs in B and G are 1 and 0 respectively. Derive the minimized state table for this FSM.

Present State	*Next state*		*Output Z*	
	W = 0	W = 1	W = 0	W = 1
A	B	C	0	0
B	D	–	0	–
C	F	E	0	1
D	B	G	0	0
E	F	C	0	1
F	E	D	0	1
G	F	–	0	–

Or

(b) Design a counter that counts pulses on line W and displays the count in the sequence.

1, 3, 7, 4, 1, 3, 7, ...

Use J.K. flip-flop.

V. (a) Design asynchronous sequential circuit to give.

(i) Output when first pulse is received and ignoring further pulses.

(ii) Output when second pulses is received and further pulses are ignored.

Or

(b) Obtain a static hazard free asynchronous circuit for the following switching function.

$F = \sum m\,(0, 3, 4, 5, 7, 8, 10, 14)$

(4 × 15 = 60 marks)